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Design and Pre-Layout Simulation of a 6-bit CMOS Pipeline ADC

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***Abstract* - This paper presents a circuit schematic level design and functional simulation of six stage, 1 bit per stage CMOS Pipeline analog to digital converter (ADC) in Cadence Virtuoso. Each stage comprises sampling, binary threshold comparison, reference selection, subtraction and nominal gain of two residue amplification. The ideal stage transfer is derived and used to clarify bit significance, code formation, and pipeline timing delay. AC, DC, and Transient simulation of schematics of operational amplifier, sample and hold circuit, comparator, residue path and cascaded stage responses. The analyzed waveforms demonstrate block level operation and stage wise bit generation at a sampling rate of 10kS/s.**

Keywords: Analog to digital converter, Cadence virtuoso, C-MOS analog circuit, pipeline ADC, residue amplifier, sample-and-hold circuit.

I. Introduction

The analog-to-digital converter circuits complete the basic requirements of digital processing system at the conversion or initial interface of the system with physical signals [1]. The pipelines ADC have advantages over the conventional topologies when a sustained conversion rate is required because conversion is divided among cascaded stages. After the initial latency the different stages works simultaneously on different sample, this advantage specifies pipeline structure from a purely sequential converter, even though it introduces residue-accuracy, interstage timing, and digital- alignment requirements [2-3].

An ideal N-bit unipolar converter maps a full-scale range V^fs into 2^N output codes. For 6-bit (N=6), there are 64 codes and the ideal significant bit interval is V^LSB = V^fs/64. Therefore, an LSB of 15.625 mV lies specifically within a 1.0V full scale range that cannot be asserted independently of the input limits. This relationship is used below to observe the code interpretation form the original simulation record counting for timing and stage delay [4-6].

The present implementation of 6-bit pipeline ADC uses six cascaded 1-bit stages. This is useful for circuit level teaching architecture as it has no decision redundancy. Practical precision pipeline pipelines commonly imply1.5-bit per stage and digital correction structure to tolerate comparator offset and incomplete settling timings [7]. The contribution of this work is therefore not a new advanced architecture rather it is a technically consistent schematic level realization, a corrected interpretation of the simulated waveforms and a verification plan that separates demonstrated behavior from performance metrics that remain to be measured. Accordingly, the reported work is presented as a per-layout functional prototype rather than a fabricated or fully characterized converter [8-9].

Lewis and Gray established the possibility of digital corrected pipeline conversion in CMOS, combining switched-capacitor residue processing with simultaneous stage operation [10]. Lewis et al. later demonstrated a nine-stage 10-bit pipeline at 20 MS/s and showcased the value of fully differential circuitry for suppressing common mode disturbances [11]. Stage resolution analysis showed that the number of bit resolved per stage trades comparator complexity against amplifier settling, capacitor matching, power, and latency. Cho and Gray resultantly demonstrated that stage scaling and relaxed comparator accuracy through digital correlation could subsequently reduce pipeline power [12].

As calibration become an important process to map for higher linearity. Lee and Song described digital domain calibration for multistep converters, while Karanicolas *et al.* demonstrated digitally self-calibrated 15-bit pipeline [16]. These works make clear that a raw set of stage decisions is not automatically an ADC output word: the decision must be delayed and aligned to the same sampled input, then combined as per the architecture. Comparator offset, finite amplifier gain, incomplete settling, capacitor mismatch, switch charge injection, clock feed through, thermal noise, and reference error all disturb the ideal residue trajectory [17].

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Against the background the present six-stage converter is best viewed as a baseline, no redundant pipeline. It is suitable for analyzing and understanding residue recursion and throughput, but quantitative claims of 6-bit accuracy require code-density spectral tests following IEEE terminology and measurement practice [18].

II. ADC Architecture

A. Ideal 1-bit stage

Let consider x^i is the input for stage indexed with (i), and have ideal condition 0 <= x^i<V_ref. The comparator decision and residue are presented by D_i, and x^(i+1) respectively.

D_i = 0, x^i < V_ref/2; D_i = 1, x^i, >= V_ref/2; (1)

x^(i=1) = 2(x^i) – D_i (V_ref) (2)

The equation (2) is expressed twice x^i for D_i = 0 and twice x^i – V_ref/2 for D_i = 1 values. In the structure of a six-stage ideal converter, the aligned decision vector [D_1, D_2….D_6] has the unsigned code and expressed in equation 3.

D = sum (i = 1 to 6) D_i 2^(6-i), 0< = D < = 63. (3)

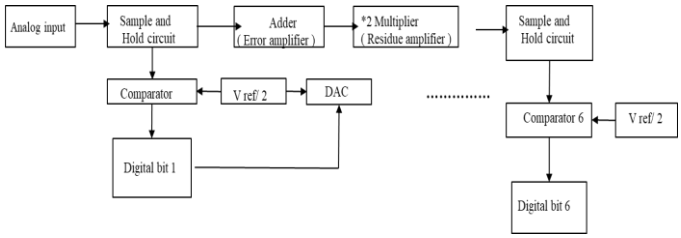

Figure 1: Functional organization of a cascaded 6-bit pipeline stages

Each stage includes an interstage sample and hold circuit and advances once per sampling period T_s, the no minimal latency of six stages is six clock cycles. At 10 kS/s, T_s = 100 microseconds and a six-cycle latency are approx. 600 microseconds. A measured analog propagation offset of about 5 micro seconds is not the pipeline latency and must not be used to link instantaneous stage outputs. Digital delay registers, or an equivalent post- processing alignment, are required so that all six stages correspond to same input sample.

III. Experimental Set Up for Simulation

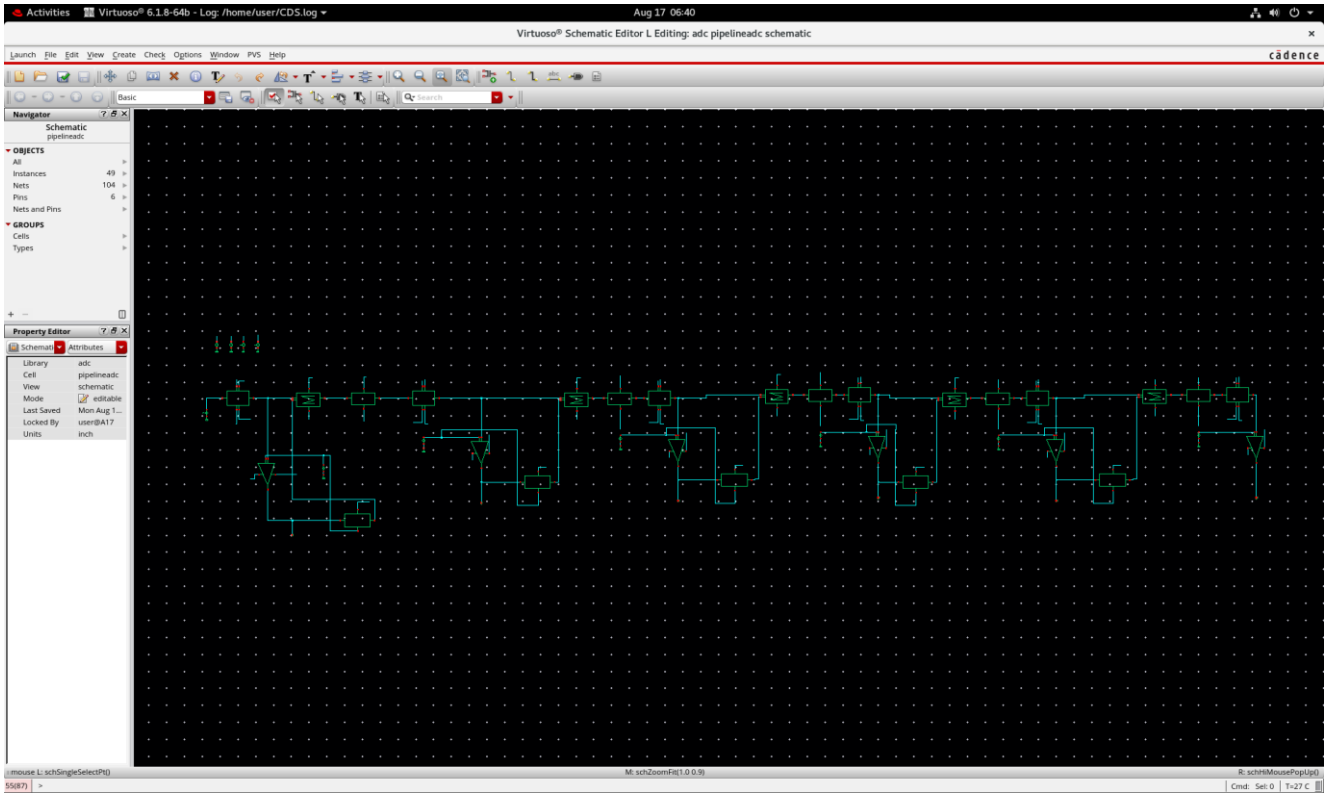

Figure 2: 6-bit pipeline ADC Schematic

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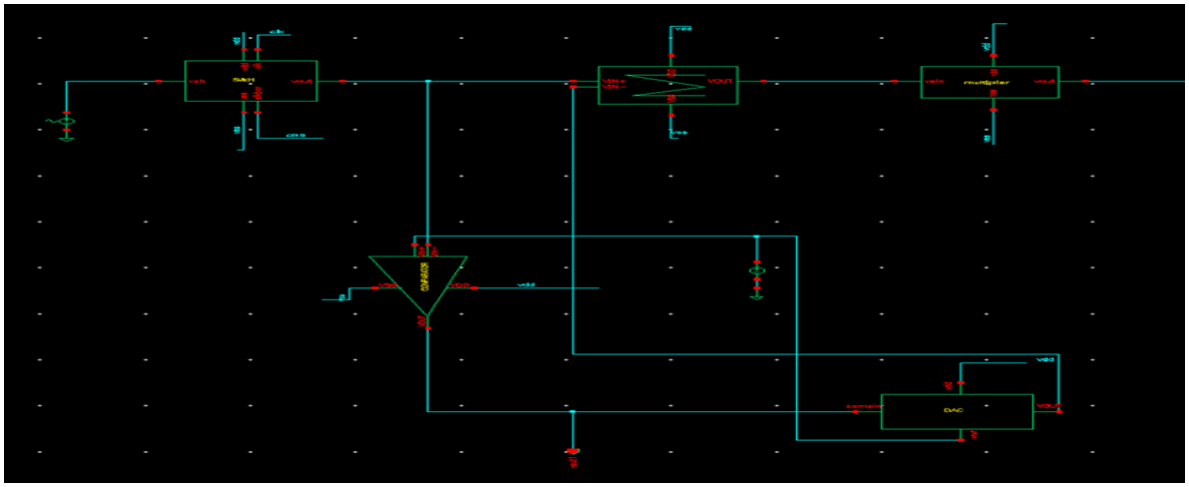

Figure 3: 1 bit pipeline ADC Schematic

Table 1: Revised Design and Simulation Conditions

Item	Value / status
Architecture	Six 1-bit stages; no redundancy
Resolution	6 bits (64 ideal codes)
Reported supply	1.8 V
Coding range used for code check	0 to 1.8 V
Ideal LSB for 1.0-V range	15.625 mV
Sampling rate	10 kS/s (T_s = 100 us)
Nominal registered latency	6 cycles (about 600 us)
Implementation status	Schematic-level, pre-layout
CMOS PDK/PDK corner	90nm CMOS/TT
Closed Loop Gain	1V/V

A. Operational and Residue Amplifiers

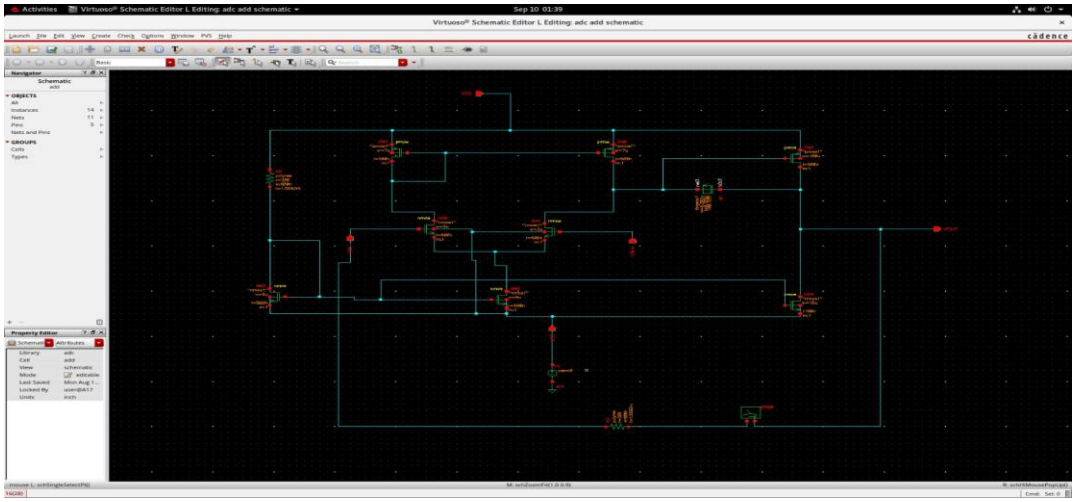

Figure 4: CMOS realization of cascaded OP amp

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The amplifier test bench is reported as a two-stage CMOS operational amplifier. For a non-inverting closed-loop residue amplifier, the correct resistive gain expression is A_CL = 1 + R_F/R_G; equal 5-kohm resistors ideally give A_CL = 1, or 0.043dB. This closed-loop residue gain is independent of the amplifier's open-loop DC gain. The original manuscript presents both reported values of 28.68 dB and 43.81 dB are not adopted as verified results owing to insufficiently defined test conditions. Phase margin should instead be obtained from a loop-gain or stability analysis under a specified feedback configuration and load condition.

B. Sampling and Decision Circuits

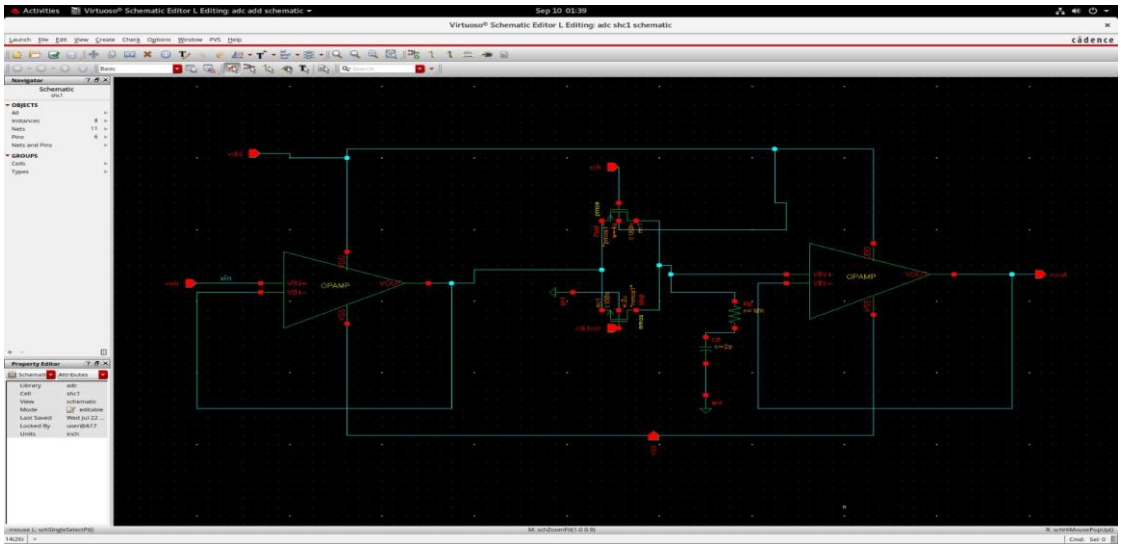

Figure 5: Sample and Hold circuit schematic using OP amp

The sample-and-hold circuit consists of a transmission gate, a hold capacitor, and a buffer. During the track mode, the transmission gate allows the input signal to be sampled by the hold capacitor. During the hold mode, the transmission gate is turned OFF, and the capacitor maintains the sampled voltage for further processing. The comparator performs differential comparison with the reference voltage, generating binary decisions for reference selection and residue generation. Transient simulations verify the sampling, comparator switching, and stage-level operation of the pipeline ADC. The comparator implements the threshold decision in (1), with its effective threshold referenced to (V_{REF}) and the input common-mode voltage. In a no redundant 1-bit stage, comparator offset shifts the decision threshold from its ideal value, directly introducing an error in the generated residue voltage consequently, offset sweeps and Monte Carlo simulations are especially important for this architecture.

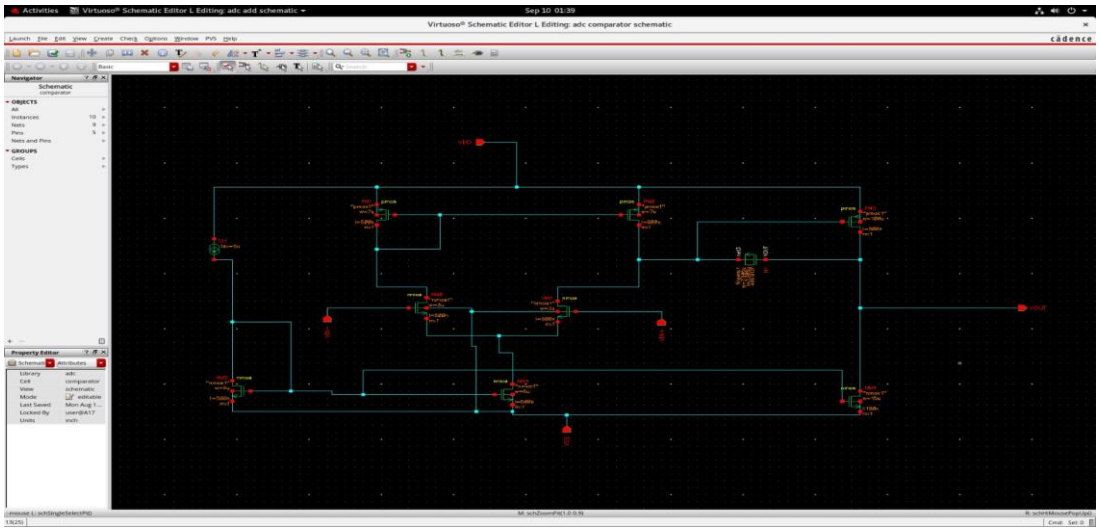

Figure 6: Comparator schematic using OP amp

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C. Reference Selection and Cascaded Stage

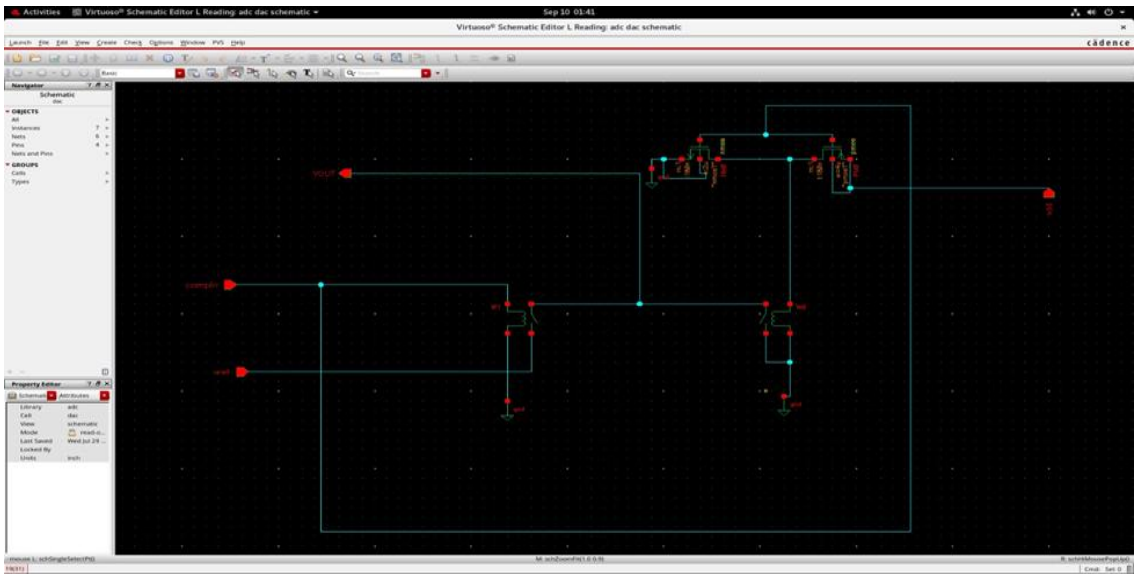

Figure 7: DAC Switch schematic

The comparator decision controls the local DAC/reference selection, followed by error amplification to generate the residue xi−di(V_REF/2). The residue amplifier provides a nominal gain of two for interstage signal propagation. For reproducibility, the final design should specify the reference levels, common-mode voltage, clock phases, transistor dimensions, capacitor values, amplifier loading, and selected PDK corner.

IV. Simulation Results and Discussion

The integral transient response shows that the cascaded stages toggles and makes different binary decisions. Although the result is a functional outcome, the simultaneously displayed traces correspond to different samples since each stage experiences a delayed residue. Thus, the vertical aggregation of six traces at a simultaneous instant is not a valid 6-bit output code on its own.

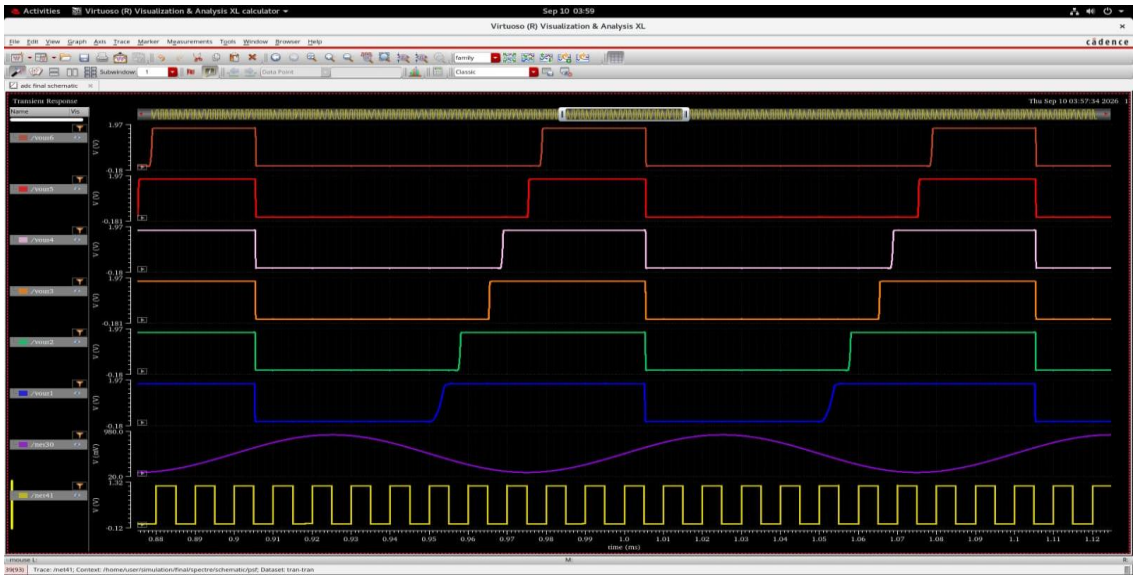

Figure 8: Integrated transient response showing the analog input and six raw stage-decision traces

The CMOS operational amplifier was characterized using AC and transient analyses, as shown in Fig. 9 and Fig. 10. The obtained frequency and time-domain responses were used for the analog processing stages.

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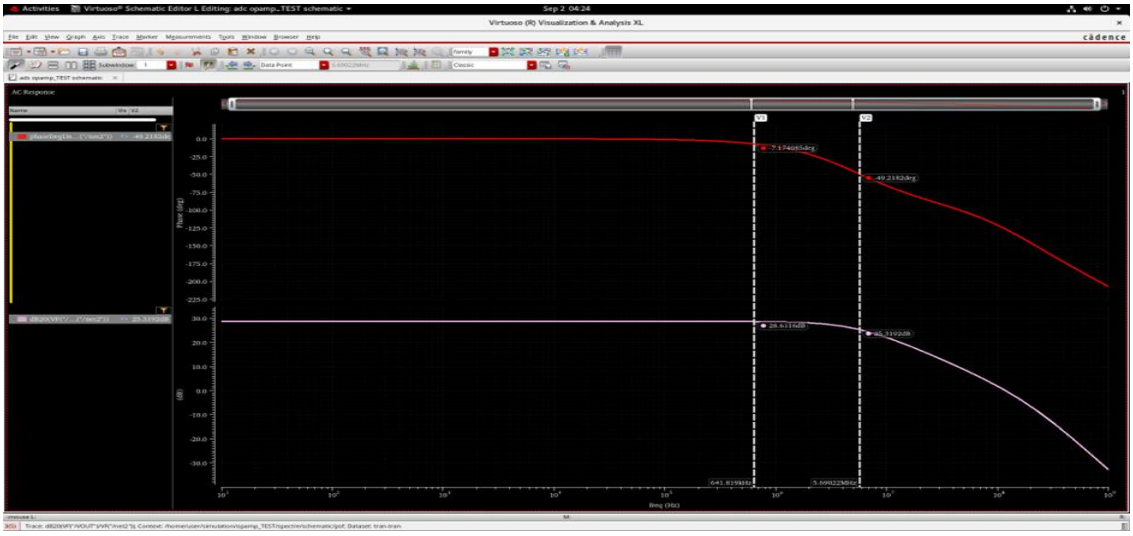

Figure 9: AC Analysis of Operational amplifier for measurement of GM, PM and working input range

Figure 10: Transient response of operational amplifier

The sample-and-hold transient in Fig. 11 verifies the sampled/held signal applied to the decision and residue paths.

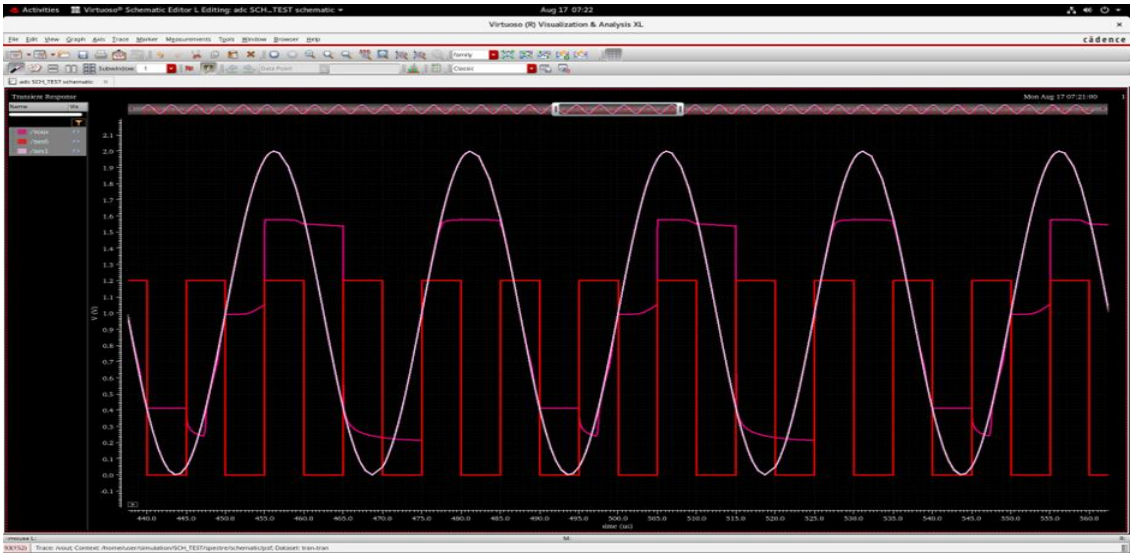

Figure 11: Transient analysis of Sample and Hold circuit

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The comparator response in Fig. 12 shows binary switching corresponding to the sampled input and reference. The resulting decision controls the reference selection and residue path.

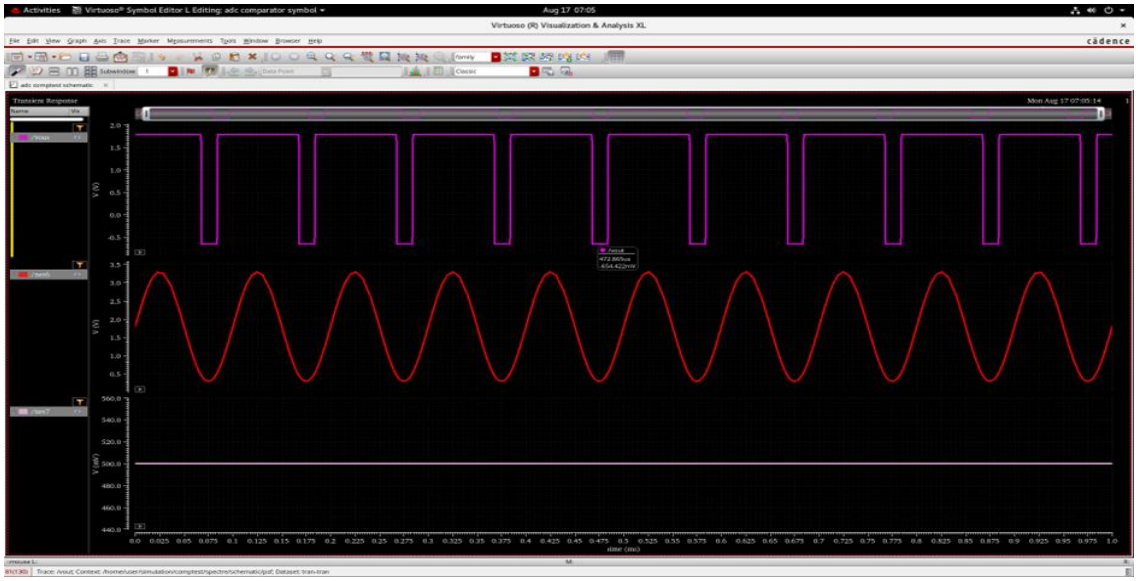

Figure 12: The transient analysis of comparator circuit

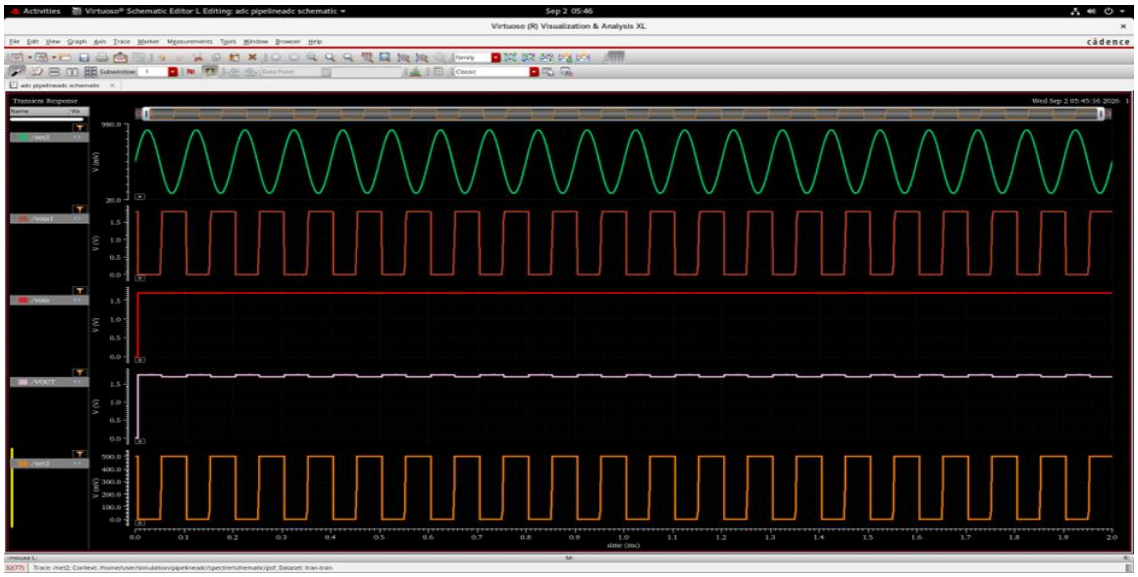

Figure 13: Transient analysis of DAC, Error amplifier and Residue amplifier

Fig. 13 presents the error-amplifier output and shows the corresponding residue-amplifier output transferred to the subsequent stage.

V. Conclusion

A 6 stage, 1 bit per stage CMOS pipeline ADC has been designed and simulated at the schematic level using Cadence virtuoso. This simulation demonstrates functional operations which includes comparator decisions and residue generation, at a sampling rate of 10kS/s. The residue amplifier was analyzed using the appropriate closed loop gain relationship; distinguish it from the amplifier open loop gain. As AC, DC and transient simulations confirm functional block level operations but they are insufficient to explain complete 6bit ADC performance. The mismatch of ideal output and final output is due to misalignment of bit and improper pipeline timing. Further improvements will include bit alignment, static and dynamic ADC characterization, and post layout verification. A 1.5 bit per stage MDAC will digitally redundancy, along with fully differential operation, non-overlapping clocks, common mode feedback, and reference buffering, may further improve the accuracy and robustness of the design.

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