Reconfigurable FIR Filter using Multipliers

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ABSTRACT - In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time. This is in contrast to infinite impulse response (IIR) filters, which may have internal feedback and may continue to respond indefinitely (usually decaying).The impulse response (that is, the output in response to a Kronecker delta input) of an Nth-order discrete-time FIR filter lasts exactly N + 1 samples (from first nonzero element through last nonzero element) before it then settles to zero.FIR filters can be discrete-time or continuous-time, and digital or analog. In this paper, FIR filter multipliers are extensively characterized with power simulations, providing a methodology for the perturbation of the coefficients of baseline filters at the algorithm level to trade-off reduced power consumption for filter quality. The proposed optimization technique does not require any hardware overhead and it enables the possibility of scaling the power consumption of the filter at runtime, while ensuring the full baseline performance of any programmed filter whenever it is required. The analyzed FIR filters were fabricated in a 28nm FD-SOI test chip and measured at a near-threshold, 600mV supply voltage.

Keywords: FIR filter, Multipliers, DSP, Bit Error Rate, IIR filter, Signal processing.

I. INTRODUCTION

An approximate computing technique on the algorithm level is proposed to reduce power consumption through switching activity reduction by carefully choosing programmable parameters of an FIR accelerator at runtime. An analysis of the switching activity of multipliers based on the number of non-zero generated partial products is presented. The dynamic power consumption of the considered multipliers has been characterized with accurate post-layout simulations, showing that the achievable power savings might differ depending on which of the two input ports is assigned to the constant coefficient. The power consumption of the multipliers contained in a programmable FIR filter is reduced by perturbing the baseline coefficients of the filter based on an extensive characterization of the implemented multiplier topology. The implementation of the power-optimized FIR filter does not require any design overhead except for the additional memory that might be required to store the perturbed coefficients.

II. EXISTING SYSTEM

The limitations and technique to perturbate the coefficients of a baseline FIR filter based on an extensive power characterization of the implemented multipliers in order to achieve dynamic power savings at the expense of a small degradation in quality. This power characterization was used to derive an algorithm that modifies the baseline filter coefficients to reduce the dynamic power consumption of the multipliers while maintaining an acceptable degradation of the filter quality. Since the proposed technique does not require any change in the design of the FIR accelerator hardware, it retains full flexibility and it allows for runtime adaptive scaling of the filter performance to trade-off power for quality. Such adaptive scaling is first demonstrated with simulations on four different multiplier designs as baseline building blocks for FIR filters. When, for example the maximum performance degradation is limited to 3dB on the filter stop band, 14.6% to 25.6% power savings are achieved in the considered FIR accelerators. The technique was further applied to two fabricated reconfigurable FIR filters, implemented as part of a 28 nm FD-SOI test chip. Silicon measurements confirmed the power benefits of the proposed technique, showing that the optimized

coefficients even result in a power reduction of 33% when compared to the baseline performance.

III. PROPOSED SYSTEM

a) Digital Filters

In a circuit one often wants to remove noise or extract useful parts of a signal, such as components lying within a certain frequency range. To do this one uses filters. There are two kinds of filters, digital and analog. Analog are build up by resistors, capacitors and op-amps. Analog filters are mathematically modeled using ordinary differential equations of Laplace transforms. They are analyzed in the time of Laplace domain. Digital filters perform numerical calculations on sampled values of a signal. Figure 1 shows how a digital filter can be used. By using an analog to digital converter (ADC) one can sample and digitized the unfiltered analog signal. The numerical calculations can then be carried out in a processor. Here the sampled signal is typically multiplied with some coefficients and added together. If an analog output is wanted a digital to analog converter (DAC) can be used as shown in figure 1.
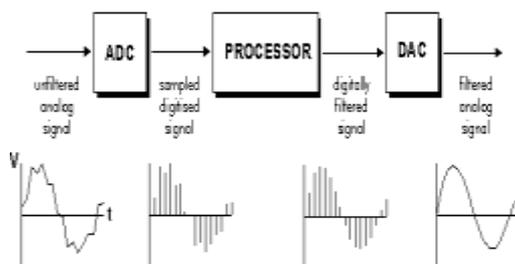

Figure-1: Basic setup of digital filters

Advantages and disadvantages

- Digital filters can realize characteristics that is not so easily done by analog filters
- Digital filters have the potential to attain a much better signal-to-noise ratio.
- Digital filters are much easier to design, test and implement than an analog filters.
- Digital filters can handle low frequency signals accurately

- Digital storage and computation limitations will give deterministic quantization errors after the ADC stage.
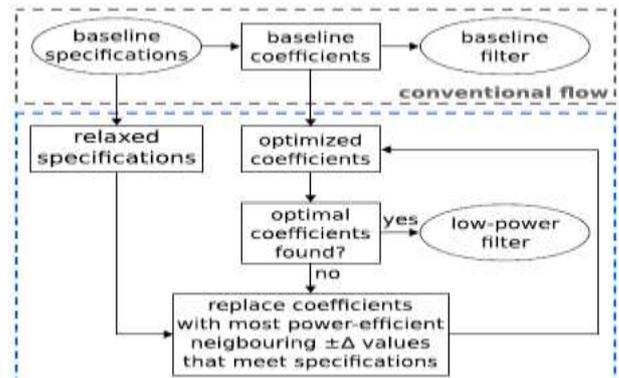

Figure-2: Flowchart of the conventional flow and proposed technique for the design of the filter

b) Transposed Direct Form of an FIR Filter

As shown in Figure 3, FIR filtering operation performs the weighted summations of input sequences, called as convolution sum, which are frequently used to implement the frequency selective low-pass, high-pass, or band-pass filters .Generally, since the amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of multipliers, significant power savings can be achieved. However, performance degradation should be carefully considered when we change the filter order.
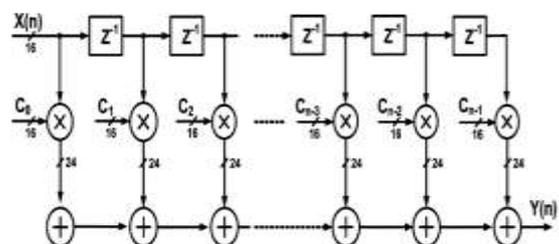

Figure-3: Transposed direct form of an FIR filter

In the fixed point arithmetic of FIR filter, full operand bit-widths of the multiplier outputs is not generally used. In Other words, as shown in Figure 3, when the bit-widths of data inputs and coefficients are 16, the multiplier generates 32-bit outputs .However,

considering the circuit area of the following adders, the LSBs of multipliers outputs are usually truncated or rounded off, (e.g., 24 bits are used in Figure 3,which incurs quantization errors. When we turn off the multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers is as small as the quantization error, filter performance degradation can be made negligible. By threshold, we mean that when the filter input and coefficient are smaller than and, respectively, the multiplication is canceled in the filtering operation. When we determine the trade-off between filter performance and power savings should be carefully considered.

c) Architecture of Proposed Reconfigurable FIR Filter

In this section, we present direct form (DF) architecture of the reconfigurable FIR filter, which is shown in Figure 4. In order to monitor the amplitudes of input samples and cancel the right multiplication operations, amplitude detector (AD) in Figure 4 is used. When the absolute value of x(n) is smaller than the threshold , the output of AD is set to "1". The design of AD is dependent on the input threshold, where the fan-in's of AND and OR gate are decided by a simple comparator. In the proposed reconfigurable filter, if we turn off the multiplier by considering each of the input amplitude only, then if the amplitude of input abruptly changes for every cycle, the multiplier will be turned on and off continuously, which incurs considerable switching activities. Multiplier control signal decision window (MCSD) in Figure 4 is used to solve the switching problem. Using ctrl signal generator inside MCSD, the number of input samples consecutively smaller than threshold are counted and the multipliers are turned off only when consecutive input samples are smaller than threshold. As an input smaller than threshold comes in and AD output is set to "1", the counter is counting up. When the counter reaches, the ctrl signal in the figure changes to "1", which indicates that consecutive small inputs are monitored and the multipliers are ready to turn off. One additional bit, in Figure 4, is added and it is controlled by ctrl. The accompanies with input data all the way in the following flip-flops to indicate that the input sample is smaller than

threshold and the multiplication can be canceled when the coefficient of the corresponding multiplier is also smaller than threshold.
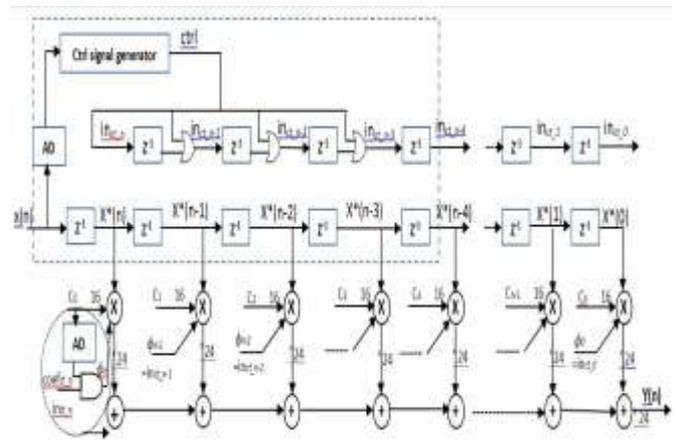
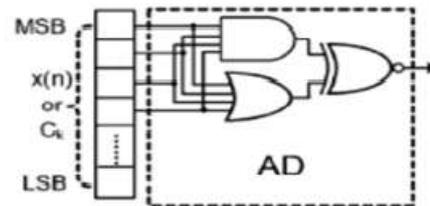

Figure-4(a): Proposed Reconfigurable fir filter

Figure-4(b): Amplitude Detection Logic (AD)

Once the signal is set inside MCSD, the signal does not change outside MCSD and holds the amplitude information of the input. A delay component is added in front of the first tap for the synchronization between and in Figure 4 since one clock pulse is needed due to the counter in MCSD. In case of adaptive filters, additional ADs for monitoring the coefficient amplitudes are required as shown in Figure 4. However, in the FIR filter with fixed or programmable coefficients, since we know the amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed. When the amplitudes of input and coefficient are smaller than threshold, the multiplier is turned off by setting signal [Figure 4] to "1". The area overheads of the proposed reconfigurable filter are flip-flops for signals, AD and ctrl signal generator in-side MCSD and the modified gates for turning off multipliers. Those overheads can be implemented using simple logic gates, and a single AD

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is needed for input monitoring as specified in Figure 4. Consequently, the overall circuit overhead for implementing reconfigurable filter is as small as a single multiplier. In the proposed architecture, go for Vedic multiplier from normal multiplier shown in fig for getting better power and speed.

IV.CONCLUSION

In Future measurements confirm the expected benefits of the proposed technique on both fabricated FIR accelerators. The power consumption of each of the accelerators with both the baseline (P base) and optimized coefficient operands (Popt) for each filter type as well as the total power savings (SF). Considering the implementation of the low-pass filter as an example, the proposed technique is able to reduce the power of the baseline filter from 335.6µW to 224.1µW for the FIR accelerator with BW2 multipliers and from 328.7µW to 218.2µW for the FIR accelerator with BR4 multipliers. The architectures implementing the digital processing platforms and control for Internet of things applications. It will provide a review of the state of the art Ultra-Low-Power (ULP) micro-controllers architecture, highlighting main challenges and perspectives, introducing the potential of exploiting parallelism in this field currently dominated by single issue processors ultra-low-power digital architectures for the internet of things.

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