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Low-Power Split-Radix FFT Processors Using Dual Edge Triggered Flip Flop

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Abstract* - Well-known Fast Fourier Transform (FFT) is the most common signal processing algorithm for observing the frequency contents of incoming signals in telecommunication transceivers. It is notably used in cognitive or software defined radio which usually demands for monitoring the spectrum in a wide frequency band. This may imply heavy computation burde non processors when the ordinary FFT algorithm is implemented, and hence yield considerable power consumption. Split-radix fast Fourier transform (SRFFT) is an ideal candidate for the implementation of a low-power FFT processor, because it has the lowest number of arithmetic operations among all the FFT algorithms. In the design of such processors, an efficient addressing scheme for FFT data as well as twiddle factors is required. The signal flow graph of SRFFT and the radix-2 FFT is same. Therefore, the generation of conventional address of FFT could also be applied to Split-radix fast Fourier transform (SRFFT). Dual edge triggered flip flop (DETFF) instead of using single edge triggered flip flop traditionally in the architecture improves speed level and decreases power consumption by using DETFF, it propagate and captures the data at both clock edges hence it is suitable for high speed of FFT module can be increased the high data rate applications.

Keywords: Address Generation, Low Power, Radix-2, Split-Radix Fast Fourier Transform (SRFFT), Twiddle Factors, Dual Edge Triggered Flip Flop (DETFF).

I. INRODUCTION

Along with the increasing demand for radio technology related services, the issue of developing techniques for utilizing available radio-frequency bands optimally is currently an important research topic. Furthermore, the techniques are being developed with the purpose of preventing interferences, which may reduce the data throughput and channel reliability in wireless networks [1].

a) Fast Fourier Transform (FFT)

Several methods for computing the Discrete Fourier Transform (DFT) efficiently are presented.

Basically, the computational problem sequence *{X (k)}* of N complex-valued numbers given another sequence of data *{x (n)}* of length N, according to the following formula:

$$X(K) = \sum_{x=0}^{N-1} X(n) W_N^{kn}, 0 \le K \le N-1$$

$$W_N = e^{-j2\pi/N}$$

b) FFT Algorithms

The decimation in time (DIT) and decimation in frequency (DIF) are the two functionally equivalent forms in FFT algorithm [2]. Both are the DFT decomposition of processing through r sample computational units and reducing the computational complexity of DFT from *O (N 2)* to *O (N log (N)).*

II. EXSITING SYSTEM

a) Split-Radix Fast Fourier Transform

Split-radix fast Fourier transform (SRFFT) is an ideal low-power FFT processor. it shows Split-radix fast

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Fourier transforms (SRFFT) can be developed by using butterfly unit of modified radix-2 system and the lowest no. of arithmetic operations using all algorithms has FFT algorithms [3], [4]. The butterfly unit exploits to save dynamic power at the expense of using more hardware resources the multiplier-gating technique. In addition, two novel address generation algorithms for both the trivial and nontrivial twiddle factors are developed [5].

b) Shared-Memory Architecture

The Split-radix fast Fourier transform (SRFFT) has forbids any conventional address generation algorithm and mixed-radix algorithm leads to the irregular locations of twiddle factors.

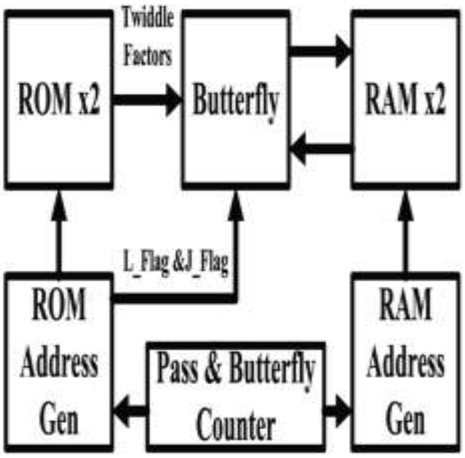

Figure-1: Shared-Memory Architecture

For split-radix FFT, it conventionally involves uneven latencies and makes scheduling difficult an L-shaped butterfly data path whose irregular shape has uneven latencies and makes scheduling difficult [6]-[8]. In this brief, we show that the SRFFT can be computed by using a modified radix-2 butterfly structure.

III. PROPOSED SYSTEM

a) Dual Edge Triggered Flip flop

Explicit-pulsed dual-edge triggered sense-amplifier flip-flop has led to an improved common mode rejection ratio. Redundant transitions are eliminated by using discharge conditional technique. Normally a design consists of combination of combinational circuit and sequential circuit. Dual edge-triggered flip flops are suitable for low-power designs since they effectively enable a halving of the clock frequency [9]. That is the main advantage of DETFF is it maintains a constant throughput only at half the clock frequency. A single-edge triggered flip flop can be implemented by two latches in series; a double edge triggered flip flop can be implemented by two latches in parallel.

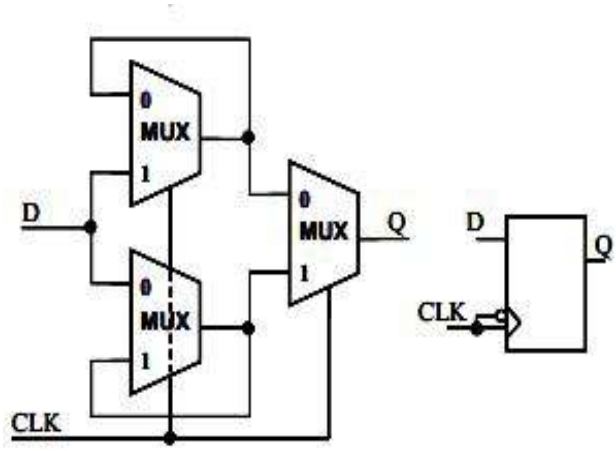

Figure-2: Description of Basic Double Edge Triggered D – Flip Flop

b) Dual Edge Triggered Flip Flop Clock Pulse

In digital system, synchronous circuits operates depend on the synchronous clock. The clock provided to the circuit at regular interval of time. The clock is the major power consumer in the design. By utilizing the clock power and time can be reduced which will be result in operating speed and reducing delay. The clock skew is the major problem which arises at large number of input design. In that case buffers are used to overcome the problem. In the DETFF it can use to capture data at both positive edge and negative edge of clock.

c) Split-Radix FFT Architecture

The algorithm originates basically from the radix-2 algorithm diagram which is transformed quite straightforwardly into a radix-4 algorithm by changing the exponents of the twiddle factors.

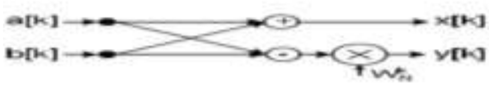

Figure-3(a): The Structure of Radix-2

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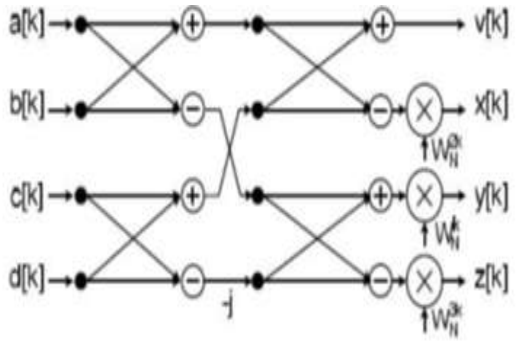

Figure-3(b): The Structure of Radix-4

d) A Power Efficient SRFFT Processor

This processor comprises a finite state machine (FSM) as a control unit, a butterfly engine, two pairs of RAMs with single address ports for real and imaginary components of the signal, a ROM for storing the twiddle factors and several interconnect units. The main difference between FFT and SRFFT is the shape of butterflies and the number of butterflies that are calculated in each stage.

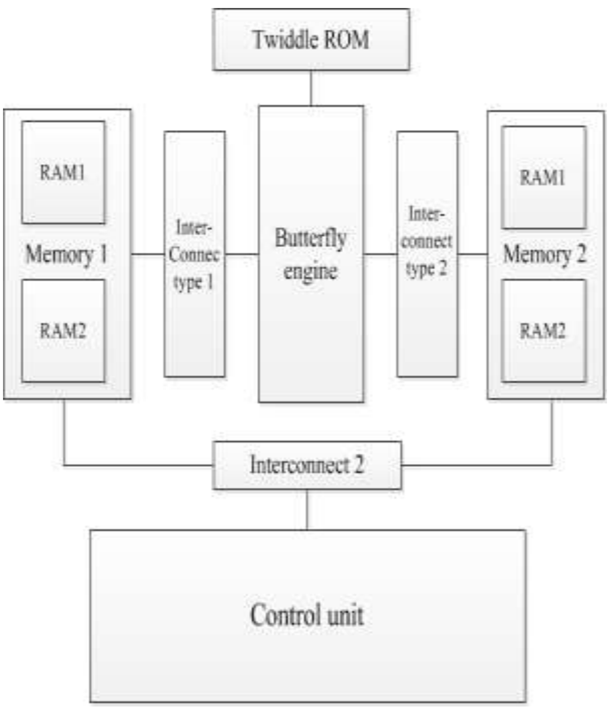

Figure-4: Architecture of the proposed SRFFT

IV. RESULT

The proposed system is a shared-memory-based SRFFT processor with DETFF. Proposed method has expense of more hardware resources and reduces power consumption. Here there are two addressing methods for both the trivial and nontrivial twiddle factors. Since SR flip flop has the minimum no. of multiplications compared with other types of flip flops, the results could be more optimal in the sense of floating point operations. This proposed system has low power consumption and increase the speed of the process.

V. CONCLUSION

In this system is used in Digital Signal Processing of Fast Fourier Transform method to improve the running process& Speed A shared-memory-based SRFFT processor with DETFF is proposed The proposed method reduces the power consumption at the expense of more hardware resources Since SRFFT has the minimum number of multiplications compared with other types of FFT, the results could be more optimal in the sense of floating point operations.

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