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Modeling of CMOS-MTJ Hybrid Full Adder Circuit for Ultra-Low Power Architectures

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Abstract - ***A novel design of adiabatic CMOS-MTJ hybrid full adder circuit is designed in this paper. Low power designs are essential with the increasing demand of IOT based portable devices in the market. Logic in memory architecture using spintronic devices along with multi-threshold CMOS circuits is an innovative idea to reduce the usual static and dynamic power dissipation in VLSI circuits. Magneto Electric Magnetic Tunnel Junction (ME MTJ) is an emerging spintronic technology, which shows good compatibility with VLSI circuits. This emerging technology is of great interest to overcome the issues such as volatility, power consumption, switching delay etc. Thus, we propose a 14T Multi-threshold CMOS & Magneto-electric MTJ hybrid full adder circuit. The circuit is simulated using National Instruments CIRCUIT DESIGN SUIT. The proposed adiabatic MT CMOS-ME MTJ full adder circuit can replace traditional 28T full adder circuit and enables logic in memory architecture in ultra-low power applications.***

***Key Words*:** CMOS, MTJ, Spintronics, Full adder, Multi-threshold, VLSI

I. INTRODUCTION

As the technology expands, the necessities for high performance devices are increasing. The developing VLSI and spintronic technologies help to achieve fast operations. During the past 40 years, semiconductor VLSI IC industry has shown a remarkable enhancement in performance, reduction in chip size as well as the speed and integration density of IC's. Exploitation of a billion transistor capacity of a single VLSI IC requires new system pattern and significant modifications to design productivity [1]. The electronic devices at the heart of such products need to reduce the power dissipation in order to conserve battery life. Consequently power consumption is a drastic problem for all integrated circuits designed today. In the last decade, internet of thing (IOT) devices and portable electronics has increased vastly [2]. Most of these devices are battery operated and thus power consumption has become a critical design constrain. Therefore, researches were established to discover new methods for designing low-power electronics [3].

The researchers came up with a method that uses non- conventional CMOS devices and nanotechnologies to reduce the leakage power consumption. Some new emerging technologies are very appropriate to be utilized in low power applications. Another technique for reducing the dynamic power consumption is to recover the stored energy instead of dissipating it as heat. This approach which operates based on energy recovery is known as adiabatic circuit design [4]. Ultra-low power architectures can be realized by logic-in-memory (LiM) paradigm, where memory elements are distributed over logic circuits. Magnetic tunnel junction (MTJ) is a nonvolatile memory that has short access time, small dimensions and compatible with CMOS technology. Therefore, it is most suited to use in logic-in-memory architectures [5]. LiM structures using MTJs are very appropriate to low power designs, because the static power dissipation is almost zero in these circuits. MTJ with CMOS design provides non-volatility along with power conservation.

II. PROPOSED SYSTEM

Full adder is a circuit that performs addition of binary numbers. A traditional full adder circuit comprises of 28 transistors. As the numbers of transistors are high, the interconnections in the circuit are high and it consumes

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large area. Thus the power consumption and switching delay is increased. Also, the major drawback is that the circuit is volatile. So as to quench these limitations to a greater extent, a 14 transistor full adder circuit design is proposed in this paper. As the numbers of interconnections are reduced, the area required is reduced [6]. Thus the switching delay and power consumption can be minimized to a greater extent. The volatility of the traditional full adder is completely eliminated by incorporating MTJ device at the output of the circuit thereby inducing memory to the device.

III. METHODOLOGY

a) Modeling of Magnetic Tunnel Junction

MTJ is essentially a magnetic storage device. It's basic structure consists of a free layer, an insulating layer and a fixed layer. The magnetic orientation of free layer is alterable, whereas that of fixed layer is constant. If the orientation of free layer and fixed layer are same, then there develops a low resistance across its terminals, indicating logic bit 0 and if the orientation seems to be different, high resistance indicating logic bit 1. These two states are used to store binary bits. This bistable state can be modeled based on the operation of a T flip-flop (Toggle flip-flop).Thus a T flip-flop based MTJ is modeled and is added to the library of the software since it is not present by default. The MTJ device structure and its footprint are shown in Figure 1 and Figure 2 respectively.

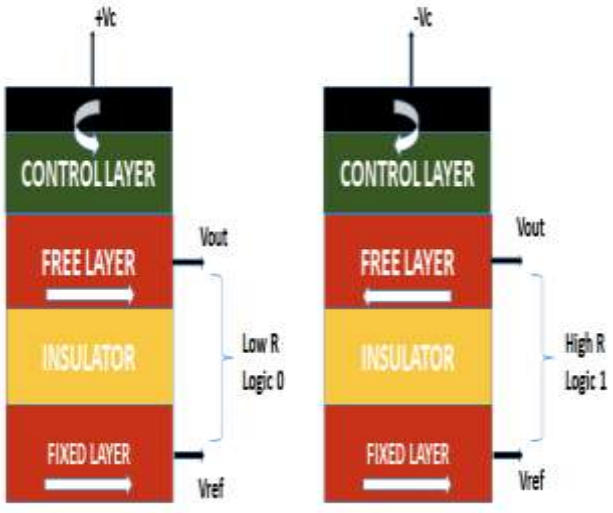
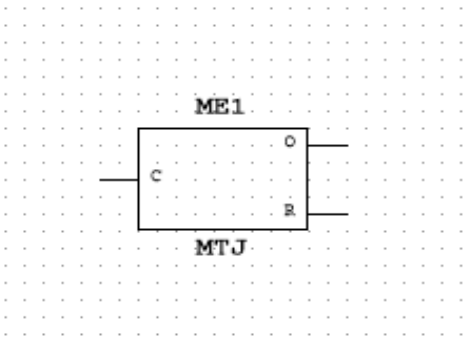


Figure 1: MTJ structure



F***igure 2: MTJ Footprint***

b) MT CMOS Full Adder

Multi- threshold CMOS comprises of transistors with different threshold voltages at the gate terminal so that they can be turned ON and OFF at desired voltages. A PMOS is turned ON whenever a voltage lowers than the threshold voltage occurs at the gate terminal whereas an NMOS is turned ON whenever a voltage higher than the threshold voltage occurs at the gate terminal. The proposed system exhibits the circuit of a 14T MT CMOS full adder. The number of transistors is reduced using multi-threshold CMOS logic thereby minimizing power consumption, switching delay and the number of interconnections. The truth table, sum circuit and carry circuit of a full adder is shown in Table 1, Figure 3 and Figure 4 respectively.

$$Sum=A\oplus B\oplus Cin$$

$$Carry = A\cdot B + A\cdot Cin + B\cdot Cin$$

TABLE I
TRUTH TABLE

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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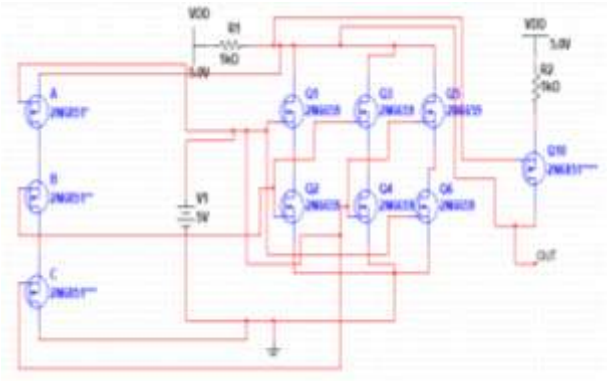

Figure-3: Sum circuit

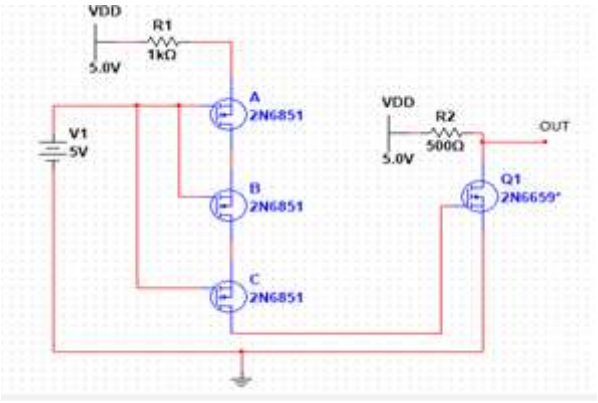

Figure-4: Carry circuit

In the proposed design, the sum circuit consists of an NMOS with 1.7255V as threshold voltage and two PMOS of threshold voltage 0V and 7mV. Similarly, the carry circuit is designed with an NMOS and PMOS of threshold voltages 2V and 0V respectively. In the truth table of a full adder, sum is high when any one of the input bit is high and when all the three input bits are high. Thus when an input bit is 1, there is a requirement for high voltage and is obtained by arranging six NMOS with threshold voltage 1.72558V in a matrix pattern. This arrangement offers high resistance and thus high voltage is obtained. If any two input bits turn out to be high, then there develops low resistance and a low voltage is obtained. When all the input bits are high, all paths are ON and very low voltage is obtained. So a multi-threshold PMOS is placed with a driving threshold of 7 mV which can be turned ON at that particular voltage to give a high voltage at the output. There occurs one more type of input, when all the bits are low, that is 000. In this case, three PMOS of threshold 0V are connected in series and output voltage is made down. Thus from this circuit we get a high output for sum when any one of the inputs is high and for all inputs high.

Considering the truth table for a full adder, the carry is high if any two inputs are high and when all inputs are high. To attain this, we have connected three PMOS with a 0 threshold voltage in series and the output is taken across a NMOS with a threshold voltage of 2V. A high voltage is achieved across the NMOS whenever the two input bits and all bits are high establishing carry output for the circuit.

c) MT CMOS - ME MTJ Hybrid Full Adder

MT CMOS - ME MTJ hybrid circuit is a blend of MT CMOS circuit with a memory device MTJ. To integrate these in a single circuit, MTJ is added in the library of NI CIRCUIT SUIT and the program code for the device is attached to the simulation tool. Now the device is completely organized to be operated in the library. MTJ and MT CMOS circuit is individually well in operation. To obtain the hybrid circuit, these have to be consolidated to a single unit. For that sum and carry circuits of full adder are combined with MTJ to achieve logic in memory architecture thereby acquiring memory capability and establishing non-volatility. The sum and carry circuits of a full adder incorporating memory device MTJ is shown in Figure 5 and Figure 6 respectively.

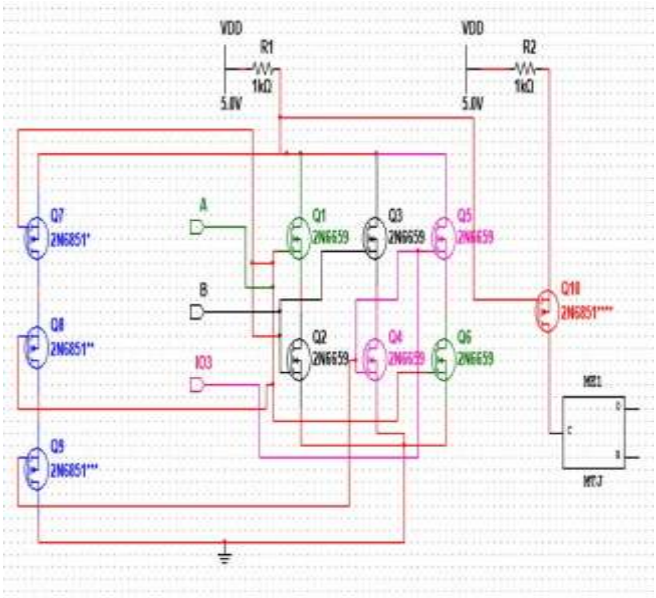

Figure-5: Sum circuit with MTJ

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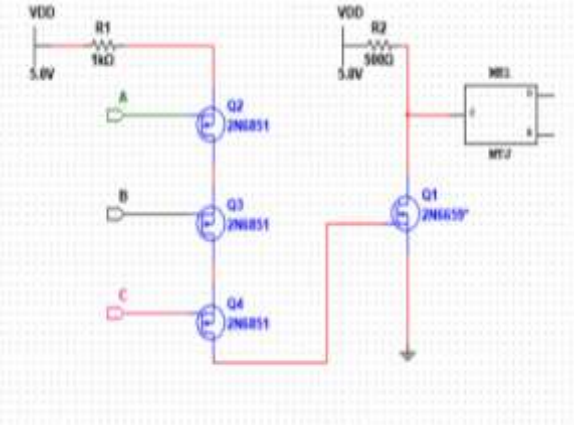

Figure-6: Carry circuit with MTJ

IV. CONCLUSION

In this paper, an advanced design of adiabatic CMOS-MTJ hybrid full adder circuit is proposed and the output is verified with the truth table. The existing design has large number of transistors, high power consumption, volatility and more number of interconnections while the proposed design quenches these disadvantages and establishes reduced number of transistors, low power consumption, less interconnections and non-volatility. The new design is suited for high-speed embedded processors where low power consumption is an essential requirement.

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