International Research Journal of Innovations in Engineering and Technology (IRJIET)

ISSN (online): 2581-3048

Volume 5, Issue 4, pp 32-41, April-2021

https://doi.org/10.47001/IRJIET/2021.504006

Coupled-Inductor and Voltage-Doubler Circuits with High Step-Up DC-DC Converter

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***Abstract* - Renewable energy sources such as photovoltaic (PV) cell and fuel cell are characterized by low output voltage, strict current ripple requirement and high output current hence they require high step up gain DC-DC converter as an important interface with the power grid or distributed generation (DG) system. High gain high efficiency DC-DC converter as a power conditioning unit for a renewable energy sources is presented here. A novel high step-up dc–dc converter with coupled-inductor and voltage-doubler circuits is proposed. The coupled-inductor and voltage-doubler circuits are integrated in the proposed converter to achieve high step up voltage gain. The converter achieves high step-up voltage gain with appropriate duty ratio and low voltage stress on the power switches. Also, the energy stored in the leakage inductor of the coupled inductor can be recycled to the output. The operating principles and the steady-state analyses of the proposed converter are discussed in detail. Finally, a prototype circuit of the proposed converter is implemented in the laboratory to verify the performance of the proposed converter.**

Keywords: Coupled inductor, high step-up voltage gain, voltage doubler.

I. INTRODUCTION

The dc–dc converter with high step-up voltage gain is widely used for many applications, such as fuel-cell energy-conversion systems, solar-cell energy-conversion systems, and high-intensity-discharge lamp ballasts for automobile headlamps. Conventional dc-dc boost converters are used for voltage step up applications. These operated at high duty ratio for achieving high voltage gain [1], [2]. High duty ratio results in serious reverse recovery problem. So, Literature says some researchers found out some converters that incur high duty ratio [3]-[11] and operates at high voltage gain among them some are transformer-less dc-dc converter include the voltage doublers type [5] and the boost type that is integrated using a switched-capacitor techniques. These converters can provide higher voltage gain than the conventional dc-dc converter. However, the voltage gain of these converters is only moderately high in above converters For high voltage gain requirements the converters must cascade more power stages which result in low efficiency. Drawbacks of the cascade converters result in efficiency low. Fly back converter is adopted to achieve high voltage gain by adjusting the turns ratio of the transformer. This converter has the merits of simple topology, easy control, and low cost, but the fact that the leakage-inductor energy of the transformer cannot be recycled results in low efficiency and high voltage stress on the active switch. In order to reduce the voltage stress, an *RCD* snubber is used. However, this decreases the efficiency.

Some active-clamp techniques are adopted to recycle the leakage-inductor energy of the transformer and to minimize the voltage stress on the active switch, but this approach requires an additional switch. Some converters, which include the clamp-mode boost type, the integrated boost–flyback type, and the integrated boost–sepic type, are developed to achieve high step-up voltage gain by using the coupled-inductor technique [6]-[11]. The leakage-inductor energy of the coupled inductor can be recycled, and the voltage stress on the active switch is reduced. Much higher voltage gain is achieved by using the coupled-inductor and the voltage multiplier or voltage-lift techniques [9]-[11].

However, the active switch will suffer high current stress during the switch-on period. A conventional high step-up dc–dc converter with a coupled inductor technique is shown in Fig.1.

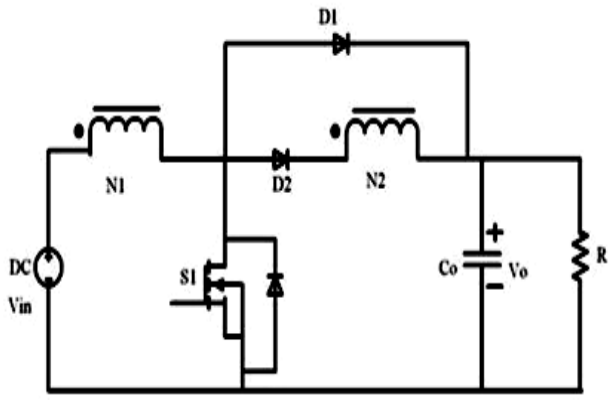

Figure 1: Conventional high step-up dc–dc converter

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The structure of this converter is very simple, and the leakage-inductor energy of the coupled inductor can be recycled to the output. However, the voltage stresses on switch S1 and diode D1, which are equal to the output voltage, are high. This paper presents a novel high step-up dc–dc converter.

II. PROPOSED CONVERTER AND OPERATION

The coupled-inductor and voltage-doubler techniques are integrated in the proposed converter to achieve high step-up voltage gain shown in Fig.2.

The features of this converter are as follows:

1) The leakage inductor energy of the coupled inductor can be recycled;

2) The voltage stresses on the switches are half the level of the output voltage; thus, the switches with low voltage rating and low ON-state resistance Rds(ON) can be selected;

3) The voltage gain achieved by the proposed converter is double that of the conventional high step-up converter; under the same voltage gain and duty ratio, the turns ratio of the coupled inductor for the proposed converter can be designed to be less than that of the conventional high step-up converter;

4) The frequency of the magnetizing-inductor current for the proposed converter is double the switching frequency. Thus, the magnetizing inductance of the coupled inductor for the proposed converter can be designed to be less than that of the conventional high step-up converter under the same switching frequency. Fig.2 shows the circuit configuration of the proposed converter, which consists of two active switches *S*1 and *S*2, one coupled inductor, four diodes *D*1−*D*4, and two output capacitors *C*1 and *C*2.

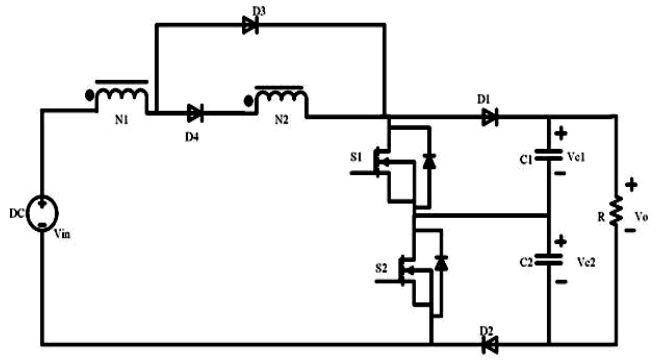

Figure 2: Circuit configuration of the proposed converter

The simplified circuit model of the proposed converter is shown in Fig. 3. The coupled inductor is modelled as a magnetizing inductor *Lm*, a primary leakage inductor *Lk*1, a secondary leakage inductor *Lk*2, and an ideal transformer. Capacitors *CS*1 and *CS*2 are the parasitic capacitors of *S*1 and *S*2, respectively. In order to simplify the circuit analysis of the proposed converter, some conditions are assumed as follows. First, all components are ideal.

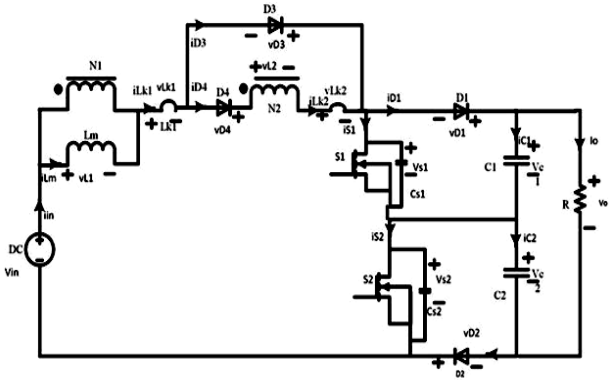

Figure 3: Simplified circuit model of the proposed converter

The ON-state resistance *R*DS(ON) of the active switches, the forward voltage drop of the diodes, and the ESR of the coupled inductor and output capacitors are ignored. Second, output capacitors *C*1 and *C*2 are sufficiently large, and the voltages across *C*1 and *C*2 are considered to be constant during one switching period.

Fig. 4 shows some typical waveforms during one switching period in continuous-conduction-mode (CCM) operation.

Modes of Operation

1) Mode I [*t*0, *t*1]: At *t* = *t*0, *S*1 and *S*2 are turned on. The Current- flow path is shown in Fig. 4a. The dc-source energy is transferred to *Lm* and *Lk*1 through *D*3, *S*1, and *S*2, so currents *iLm*, *iLk*1, and *iD*3 are increased. The energy stored in *Lk*2 is released to *Lm* and *Lk*1 through *D*4, *S*1, and *S*2. Thus, *iLk*2 is decreased. Meanwhile, the energy stored in *Lk*2 is recycled. The energy stored in *CS*2 is rapidly and completely discharged. The energies stored in *C*1 and *C*2 are discharged to the load. This mode ends when *iLk*2 is equal to zero at t=*t*1.

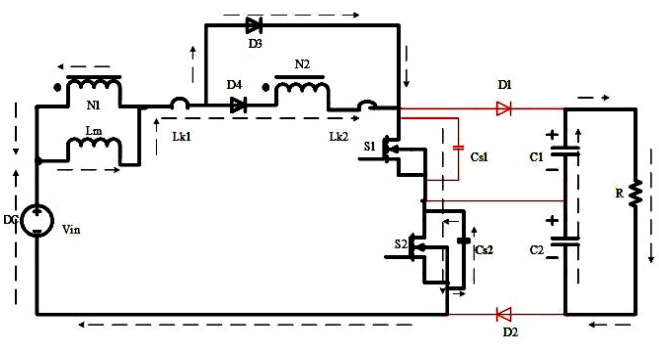

Figure 4(a): Operating mode I

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2) Mode II [*t*1, *t*2]: In this mode, *S*1 and *S*2 are still turned on. The current-flow path is shown in Fig.4b). The dc source energy is still transferred to *Lm* and *Lk*1. Thus, *iLm* and *iLk*1 are still increased. The energies stored in *C*1 and *C*2 are still discharged to the load.

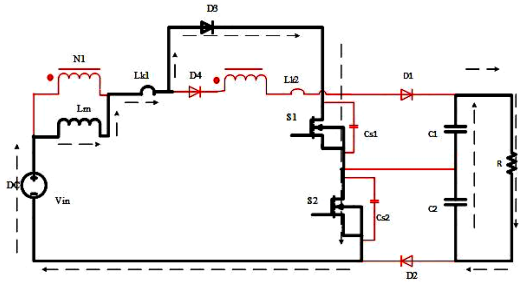

Figure 4(b): Mode II

3) Mode III [*t*2, *t*3]: At *t* = *t*2, *S*1 is turned off, and *S*2 is still turned on. The current-flow path is shown in Fig. 4(c). The dc-source energy is still transferred to *Lm*, *Lk*1, and *CS*1. Meanwhile, the voltage across *S*1 is increased rapidly. The energies stored in *C*1 and *C*2 are still discharged to the load.

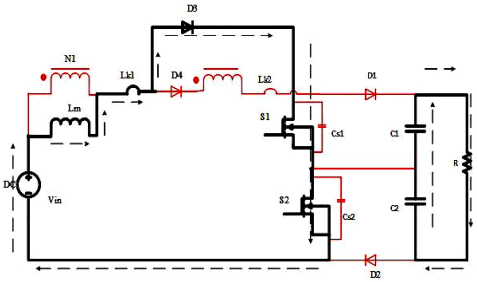

Figure 4(c): Mode III

4) Mode IV [*t*3, *t*4]: During this time interval, *S*1 is still turned off, and *S*2 is still turned on. The current-flow path is shown in Fig. 4(d). The dc source, *Lm*, and *Lk*1 are series connected to transfer their energies to *Lk*2, *C*1, and the load. Thus, *iLm* and *iLk*1 are decreased, and *iLk*2 is increased. Meanwhile, the energy stored in *Lk*1 is recycled to *C*1 and the load. The energy stored in *C*2 is still discharged to the load. This mode ends when *iLk*1 is equal to *iLk*2 at *t* = *t*4.

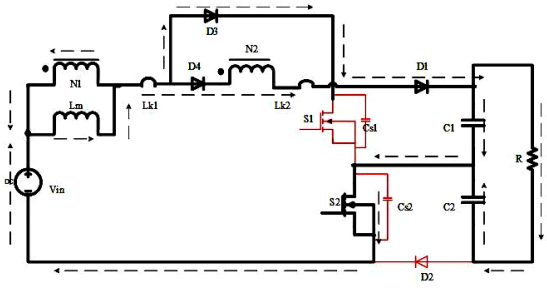

Figure 4(d): Mode IV

5) Mode V [t4, t5]: During this period, S1 is still turned off, and S2 is still turned on. The current-flow path is shown in Fig. 4(e). The dc source, Lm, Lk1, and Lk2 are series connected to transfer their energies to C1 and the load. Thus, iLm, iLk1, and iLk2 are decreased. The energy stored in C2 is still discharged to the load.

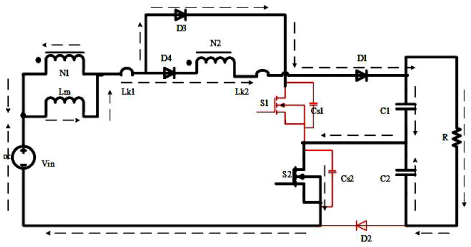

Figure 4(e): Mode V

6) Mode VI [t5, t6]: At t = t5, S1 and S2 are turned on. The current-flow path is shown in Fig. 4(f). The dc-source energy is transferred to Lm and Lk1 throughD3, S1, and S2. Therefore, currents iLm, iLk1, and iD3 are increased. The energy stored in Lk2 is released to Lm and Lk1 through D4, S1, and S2. Thus, iLk2 is decreased. Meanwhile, the energy stored in Lk2 is recycled. The energy stored in Cs1 is rapidly and completely discharged. The energies stored in C1 and C2 are discharged to the load. This mode ends when iLk2 is equal to zero at t = t6.

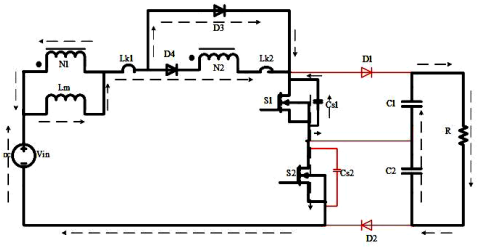

Figure 4(f): Mode VI

7) Mode VII [t6, t7]: During this time interval, S1 and S2 are still turned on. The current-flow path is shown in Fig. 5(g). The dc-source energy is still transferred to Lm and Lk1. Thus, iLm and iLk1 are still increased. The energies stored in C1 and C2 are still discharged to the load.

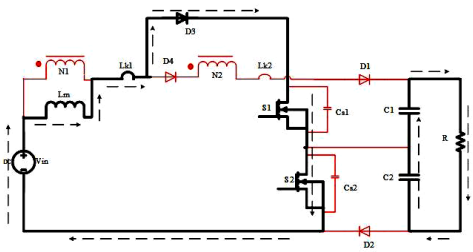

Figure 4(g): Mode VII

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8) Mode VIII [*t*7, *t*8]: At *t* = *t*7, *S*1 is still turned on, and *S*2 is turned off. The current-flow path is shown in Fig. 4(h). The dc-source energy is still transferred to *Lm*, *Lk*1, and *CS*2. Meanwhile, the voltage across *S*2 is increased rapidly. The energies stored in *C*1 and *C*2 are still discharged to the load.

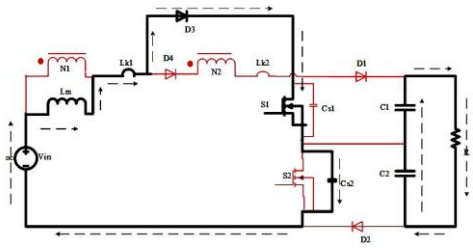

Figure 4(h): Mode VIII

9) Mode IX [*t*8, *t*9]: During this period, *S*1 is still turned on, and *S*2 is still turned off. The current-flow path is shown in Fig. 4(i). The dc source, *Lm*, and *Lk*1 are series connected to transfer their energies to *Lk*2, *C*2, and the load. Thus, *iLm* and *iLk*1 are decreased, and *iLk*2 is increased. Meanwhile, the energy stored in *Lk*1is recycled to *C*2 and the load. The energy stored in *C*1 is still discharged to the load. This mode ends when *iLk*1 is equal to *iLk*2 at *t* = *t*9.

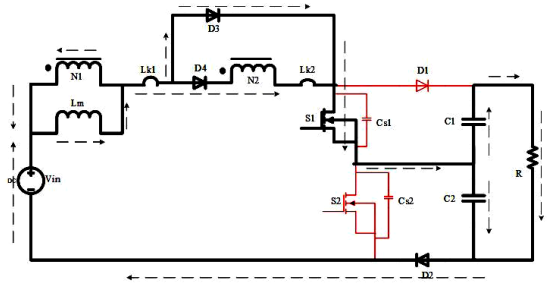

Figure 4(i): Mode IX

10) Mode X [t9, t10]: In this mode, S1 is still turned on, and S2 is still turned off. The current - flow path is shown in Fig. 4(j). The dc source, Lm, Lk1, and Lk2 are series connected to transfer their energies to C2 and the load. Thus, iLm, iLk1, and iLk2 are decreased. The energy stored in C1 is still discharged to the load. This mode ends when S1and S2 are turned on at the beginning of the next switching period.

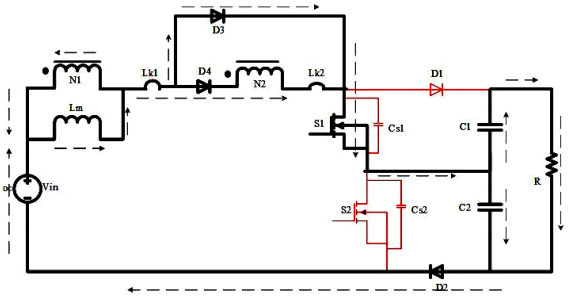

Figure 4(j): Mode X

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A) Voltage Gain

At CCM operation, the time durations of modes I, III, IV, VI, VIII, and IX are very short as compared to one switching Period. Thus, only modes II, V, VII, and X are considered. At modes II and VII, the following equations can be written from Fig. 4(b) and (g):

$$v_{L1}^{\mathrm{II}} = v_{L1}^{\mathrm{VII}} = kV_{\mathrm{in}} \tag{1}$$

$$\frac{di_{Lm}^{\mathrm{II}}}{dt} = \frac{di_{Lm}^{\mathrm{VII}}}{dt} = \frac{kV_{\mathrm{in}}}{L_m} \tag{2}$$

where the coupling coefficient k of the coupled inductor is equal to Lm/(Lm+Lk1). At mode V, the following equations are derived from Fig. 4(e):

$$i_{Lk1}^{V} = i_{Lk2}^{V} \tag{3}$$

$$i_{Lm}^{V} = (1+n)i_{Lk1}^{V} \tag{4}$$

$$V_{\mathrm{in}} - V_{c1} = v_{L1}^{V} + v_{Lk1}^{V} + v_{L2}^{V} + v_{Lk2}^{V} \tag{5}$$

where the turns ratio n of the coupled inductor is equal to N2/N1. Voltage v_{Lk2}^{V} is found to be

$$v_{Lk2}^{V} = L_{k2}\frac{di_{Lk2}^{V}}{dt} = L_{k2}\frac{di_{Lk1}^{V}}{dt} = n^2 L_{k1}\frac{di_{Lk1}^{V}}{dt} = n^2 v_{Lk1}^{V}. \tag{6}$$

Substituting (6) into (5) yields the following equation:

$$V_{\mathrm{in}} - V_{c1} = (1+n)v_{L1}^{V} + (1+n^2)v_{Lk1}^{V}. \tag{7}$$

Voltage v_{Lk2}^{V} is written as

$$v_{L1}^{V} = L_m\frac{di_{Lm}^{V}}{dt} = (1+n)L_m\frac{di_{Lk1}^{V}}{dt}. \tag{8}$$

Thus

$$v_{Lk1}^{V} = L_{k1}\frac{di_{Lk1}^{V}}{dt} = \frac{L_{k1}}{(1+n)L_m}v_{L1}^{V} = \frac{1-k}{(1+n)k}v_{L1}^{V}. \tag{9}$$

Substituting (9) into (7) yields the following equation:

$$v_{L1}^{V} = \frac{(1+n)k}{1+2nk+n^2}(V_{\mathrm{in}} - V_{c1}) \tag{10}$$

$$\frac{di_{Lm}^{V}}{dt} = \frac{(1+n)k}{1+2nk+n^2} \times \frac{V_{\mathrm{in}} - V_{c1}}{L_m}. \tag{11}$$

Similarly, at mode X, the voltage across Lm is derived from Fig. 5(j) as follows:

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$$v_{L1}^{X} = \frac{(1+n)k}{1+2nk+n^2}(V_{in} - V_{c2}) \qquad (12)$$

$$\frac{di_{Lm}^{X}}{dt} = \frac{(1+n)k}{1+2nk+n^2} \times \frac{V_{in} - V_{c2}}{L_m}. \qquad (13)$$

Using the volt–second balance principle on Lm, the following equation is derived:

$$\int_0^{\frac{DT_s}{2}} v_{L1}^{II} dt + \int_0^{\frac{(1-D)T_s}{2}} v_{L1}^{V} dt + \int_0^{\frac{DT_s}{2}} v_{L1}^{VII} dt + \int_0^{\frac{(1-D)T_s}{2}} v_{L1}^{X} dt = 0. \qquad (14)$$

Substituting (1), (10), and (12) into (14), the voltage gain is obtained as

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2(1+n-nD+n^2D+2nDk)}{(1-D)(1+n)}. \qquad (15)$$

Thus, the plot of the voltage gain versus the duty ratio under various coupling coefficients of the coupled inductor is shown in Fig. 6. It can be seen that the voltage gain is not very sensitive to the coupling coefficient. If the impact of the leakage inductor of the coupled inductor is neglected, then coupling coefficient k is equal to one. Substituting k=1 into (15), the voltage gain becomes

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2(1+nD)}{1-D}. \qquad (16)$$

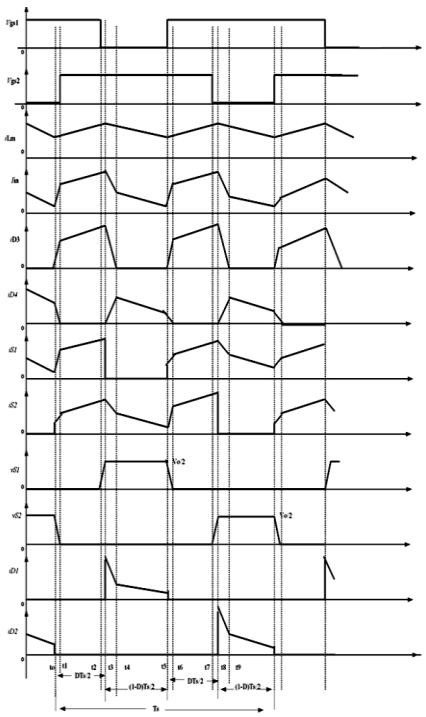

Figure 5: Some typical waveforms of the proposed converter at CCM operation

MCCM

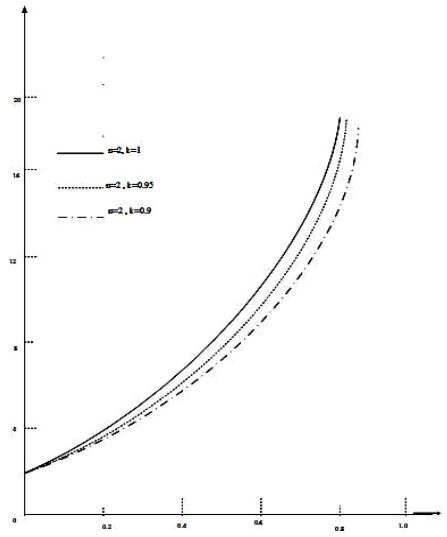

Figure 6: Voltage gain versus duty ratio of the proposed converter at CCM operation with n =2 and various values for k

B) Boundary Operating Condition

Fig. 7 shows some waveforms of the proposed converter at boundary conduction mode (BCM). When the proposed converter is operated in BCM, the peak value of the magnetizing inductor current is given as

$$I_{Lmp} = \frac{kDV_{in}T_s}{2L_m}. \qquad (17)$$

Since the time duration [t1, t3] is very short as compared to one switching period, this time duration is not considered. The average value of iD1 is found to be

$$I_{D1} = \frac{\frac{1}{2} \times \frac{I_{Lmp}}{1+n} \times \frac{1-D}{2}T_s}{T_s} = \frac{(1-D)I_{Lmp}}{4(1+n)}. \qquad (18)$$

At steady state, the average value of ID1 is equal to Io. Thus

$$\frac{(1-D)I_{Lmp}}{4(1+n)} = I_o = \frac{V_o}{R}. \qquad (19)$$

Then, the normalized magnetizing-inductor time constant is defined as

$$\tau_{Lm} \equiv \frac{L_m}{RT_s} = \frac{L_m f_s}{R} \qquad (20)$$

Where fs is the switching frequency.

Substituting (15), (17), and (20) into (19), the boundary normalized magnetizing-inductor time constant τLmB can be derived as

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$$\tau_{LmB} = \frac{kD(1-D)^2}{16(1+n-nD+n^2D+2nDk)}. \quad (21)$$

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The curve of τLmB is shown in Fig. 6. If τLm is larger than τLmB, the proposed converter is operated in CCM.

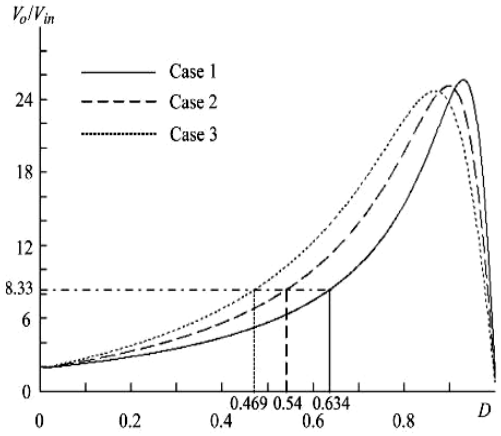

Figure 7: Calculated voltage gain versus duty ratio

C) Efficiency Analysis

In order to simplify the efficiency analysis of the proposed converter, the leakage inductors of the coupled inductor are neglected. Thus, the operating principle is divided into four modes, the equivalent circuits for which are shown in Fig. 9. r*L1* and r*L2* represent the ESRs of the primary and secondary windings of the coupled inductor. V*FD1*−V*FD4* and rD1−rD4 are the ON-state forward voltage drops and resistances of D1−D4.rS1 and rS2 denote the ON-state resistances of S1 and S2.When S1andS2 are turned on; the equivalent circuit is shown in Fig. 9(a). This time interval is DTs/2. The average values of ic1 and vL1are obtained as

$$I_{c1}^{I} = I_{c1}^{III} = -\frac{V_o}{R} \quad (22)$$

$$V_{L1}^{I} = V_{L1}^{III} = V_{in} - V_{FD3} - I_{in(on)}(r_{L1} + r_{D3} + r_{S1} + r_{S2}) \quad (23)$$

Where I*in*(on) is the average value of the input current in this time interval.

When S1 is turned off and S2 is turned on, the equivalent circuit is shown in Fig. 9(b). This time interval is (1−D)Ts/2.

The average values of ic1 and vL1 are derived as

$$I_{c1}^{II} = I_{in(off)} - \frac{V_o}{R} \quad (24)$$

$$V_{L1}^{II} = \frac{V_{in} - V_{FD4} - V_{FD1} - V_{c1} - I_{in(off)}(r_{L1} + r_{D4} + r_{L2} + r_{D1} + r_{S2})}{1+n} \quad (25)$$

Where *Iin(off)* is the average value of the input current in this time interval.

When S1 is turned on and S2 is turned off, the equivalent circuit is shown in Fig. 9(c). This time interval is (1−D)Ts/2.

The average values of ic1 and vL1 are given as

$$I_{c1}^{IV} = -\frac{V_o}{R} \quad (26)$$

$$V_{L1}^{IV} = \frac{V_{in} - V_{FD4} - V_{c2} - V_{FD2} - I_{in(off)}(r_{L1} + r_{D4} + r_{L2} + r_{S1} + r_{D2})}{1+n}. \quad (27)$$

By using the ampere–second balance principle on C1, the following equations are obtained:

$$\int_0^{\frac{DT_s}{2}} I_{c1}^{I} dt + \int_0^{\frac{(1-D)T_s}{2}} I_{c1}^{II} dt + \int_0^{\frac{DT_s}{2}} I_{c1}^{III} dt + \int_0^{\frac{(1-D)T_s}{2}} I_{c1}^{IV} dt = 0. \quad (28)$$

Substituting (22), (24), and (26) into (28),I*in(off)* can be computed as

$$I_{in(off)} = \frac{2V_o}{(1-D)R}. \quad (29)$$

Also, I*in(on)* can be found to be

$$I_{in(on)} = (1+n)I_{in(off)} = \frac{2(1+n)V_o}{(1-D)R}. \quad (30)$$

Using the volt–second balance principle on Lm yields

$$\int_0^{\frac{DT_s}{2}} V_{L1}^{I} dt + \int_0^{\frac{(1-D)T_s}{2}} V_{L1}^{II} dt + \int_0^{\frac{DT_s}{2}} V_{L1}^{III} dt + \int_0^{\frac{(1-D)T_s}{2}} V_{L1}^{IV} dt = 0. \quad (31)$$

Substituting (23), (25), and (27) into (31), the actual voltage gain is derived as

$$\frac{V_o}{V_{in}} = \frac{2(1+nD)}{1-D} \times \frac{1-A_1}{1 + \frac{4D(1+n)^2A_2}{(1-D)^2R} + \frac{2A_3}{(1-D)R}} \quad (32)$$

Where

$$A_1 = \frac{1-D}{2(1+nD)}\left(\frac{V_{FD1}}{V_{in}} + \frac{V_{FD2}}{V_{in}}\right) + \frac{(1+n)D}{1+nD} \times \frac{V_{FD3}}{V_{in}} + \frac{1-D}{1+nD} \times \frac{V_{FD4}}{V_{in}}$$

$$A_2 = r_{L1} + r_{D3} + r_{S1} + r_{S2}$$

$$A_3 = 2r_{L1} + 2r_{L2} + r_{D1} + r_{D2} + 2r_{D4} + r_{S1} + r_{S2}.$$

International Research Journal of Innovations in Engineering and Technology (IRJIET)

ISSN (online): 2581-3048

Volume 5, Issue 4, pp 32-41, April-2021

https://doi.org/10.47001/IRJIET/2021.504006

The input power and output power of the proposed converter are obtained as

$$P_{\text{in}} = V_{\text{in}} I_{\text{in(on)}} \left(\frac{D}{2} + \frac{D}{2}\right) + V_{\text{in}} I_{\text{in(off)}} \left(\frac{1-D}{2} + \frac{1-D}{2}\right) \quad (33)$$

$$P_o = \frac{V_o^2}{R}. \quad (34)$$

Substituting (29) and (30) into (33), the input power can be computed as

$$P_{\text{in}} = \frac{2(1+nD)}{(1-D)R} V_{\text{in}} V_o. \quad (35)$$

From (32), (34), and (35), the efficiency of the proposed converter is found to be

$$\eta = \frac{P_o}{P_{\text{in}}} = \frac{1-A_1}{1 + \frac{4D(1+n)^2 A_2}{(1-D)^2 R} + \frac{2A_3}{(1-D)R}}. \quad (36)$$

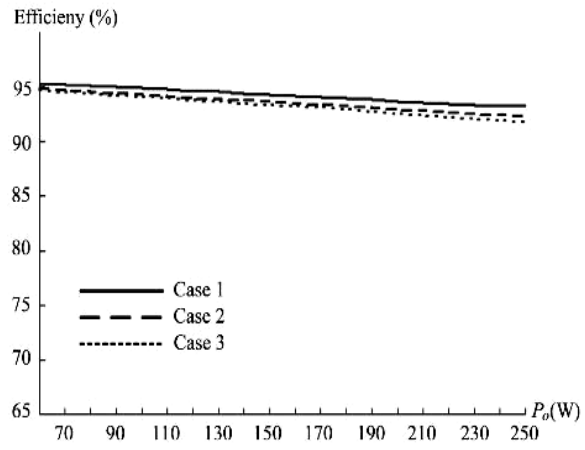

Figure 8: Calculated efficiency versus output power

D) Voltage and Current Stresses on Power Devices

According to the operating principle, the voltage and current stresses on power devices are discussed as follows. If the impact of the leakage inductor of the coupled inductor is ignored, the voltage stresses on *S1*, *S2*, and *D1*−*D4* are given as

$$V_{S1} = V_{S2} = V_{D1} = V_{D2} = \frac{V_o}{2} \quad (37)$$

$$V_{D3} = \frac{n}{1+n}\left(\frac{V_o}{2} - V_{\text{in}}\right) \quad (38)$$

$$V_{D4} = nV_{\text{in}}. \quad (39)$$

From (2), the ripple of i*Lm* can be derived as

$$\Delta I_{Lm} = \frac{kDV_{\text{in}}T_s}{2L_m}. \quad (40)$$

From (29), (30), and (40), the current stresses that flow through *S1*,*S2*, and *D1*−*D4* are found to be

$$I_{S1} = I_{S2} = I_{D1} = I_{D2} = I_{D3} = I_{\text{in(on)}} + \frac{\Delta I_{Lm}}{2} = \frac{2(1+n)V_o}{(1-D)R} + \frac{kDV_{\text{in}}T_s}{4L_m} \quad (41)$$

$$I_{D4} = I_{\text{in(off)}} + \frac{\Delta I_{Lm}}{2(1+n)} = \frac{2V_o}{(1-D)R} + \frac{kDV_{\text{in}}T_s}{4(1+n)L_m}. \quad (42)$$

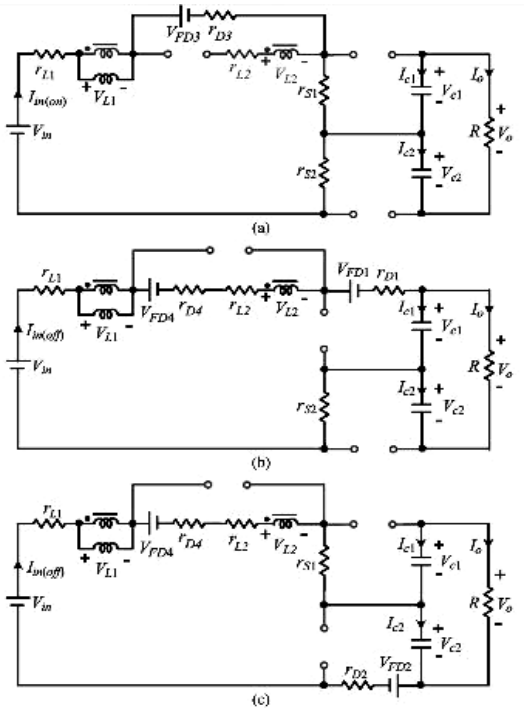

Figure 9: Equivalent circuit of the proposed converter, including the ESR of the coupled inductor, the ON -state forward voltage drop and resistance of the diodes, and the ON -state resistance of the switches (a) S1 and S2 on

(b)S1 off and S2 on. (c)S1 on and S2 off.

Case 1) $n = 1$, $r_{L1} = r_{L2} = r_{D1} = r_{D2} = r_{D3} = r_{D4} = 10$ mΩ, $r_{S1} = r_{S2} = 18$ mΩ, $V_{FD1} = V_{FD2} = 0.92$ V, and $V_{FD3} = V_{FD4} = 0.75$ V.

Case 2) $n = 2$, $r_{L1} = r_{D1} = r_{D2} = r_{D3} = r_{D4} = 10$ mΩ, $r_{L2} = 20$ mΩ, $r_{S1} = r_{S2} = 18$ mΩ, $V_{FD1} = V_{FD2} = 0.92$ V, and $V_{FD3} = V_{FD4} = 0.85$ V.

Case 3) $n = 3$, $r_{L1} = r_{D1} = r_{D2} = r_{D3} = r_{D4} = 10$ mΩ, $r_{L2} = 30$ mΩ, $r_{S1} = r_{S2} = 18$ mΩ, $V_{FD1} = V_{FD2} = 0.92$ V, and $V_{FD3} = V_{FD4} = 0.85$ V.

Substituting the circuit specifications and parameters into (32) and (36), the calculated voltage gain and efficiency are shown in Figs. 7 and 8. Fig. 8 shows that the calculated efficiency in case 1 is better than those in cases 2 and 3. Thus, the turns ratio n of the coupled inductor is chosen as one.

International Research Journal of Innovations in Engineering and Technology (IRJIET)

ISSN (online): 2581-3048

Volume 5, Issue 4, pp 32-41, April-2021

https://doi.org/10.47001/IRJIET/2021.504006

As can be seen from Fig. 11, duty ratio D is 0.634 for case 1. Substituting k=1, n=1, and D=0.634 into (21), the boundary normalized magnetizing-inductor time constant τLmB is obtained as 0.00162. The proposed converter is operated in CCM from 25% of the full load, i.e., R = 640 Ω. When τLm is larger than τLmB, the proposed converter is operated in CCM. Using (20), Lm is found by

$$\tau_{Lm} = \frac{L_m f_s}{R} = \frac{L_m \times 25k}{640} > 0.00162$$

$$L_m > 41\ \mu H.$$

Lm is selected to be 48μH

IV. SIMULATION RESULTS

A Simulation of the proposed converter was modelled with the circuit parameters as follows:

Table 1: Circuit parameters

Capacitors C1,C2	47uF
Resistor R	160 Ω
MOSFETs	IXFK140N20P
Diodes D1,D2	MBR20150CT
Diodes D3,D4	SBL2060CT
Inductor Lm	48uH

And circuit specifications are shown below

Table 2: Circuit specifications

parameters	specifications
Vin	24v
Vo	200v
fs	25kz
Po	250w
Vdss	200v
Rds(on)	18mohm
Vrrm(D1,D2)	150v
Vf(D1,D2)	0.92v
Vrrm(D3,D4)	60v
Vf(D3,D4)	0.75v
Duty ratio(D)	0.634
Turns ratio(n)	1

The below are the simulation results obtained by considering all the circuit parameters and specifications.

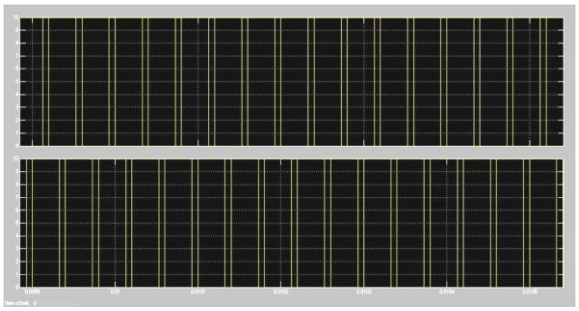

Figure 10: Waveforms of the gate pulses of the switch s1& s2

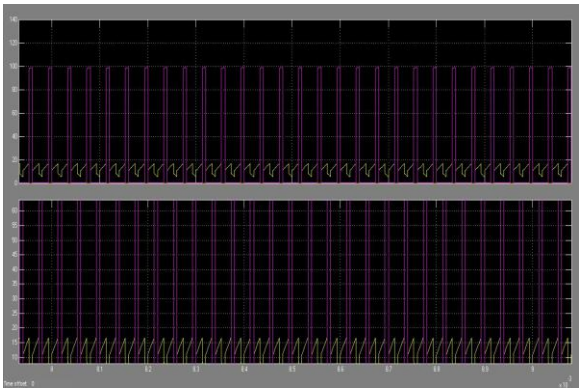

Figure 11: Voltage and current waveforms of switch s1 & s2

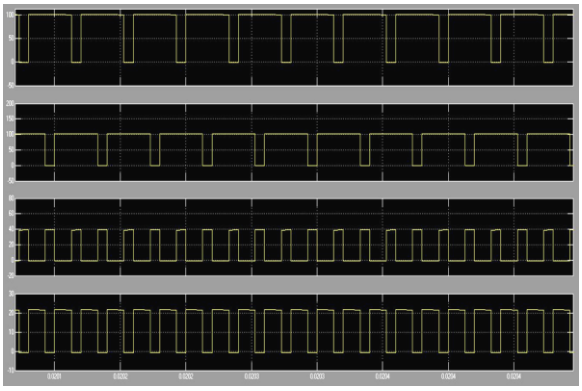

Figure 12: Voltage waveform of diode D1, D2, D3, D4

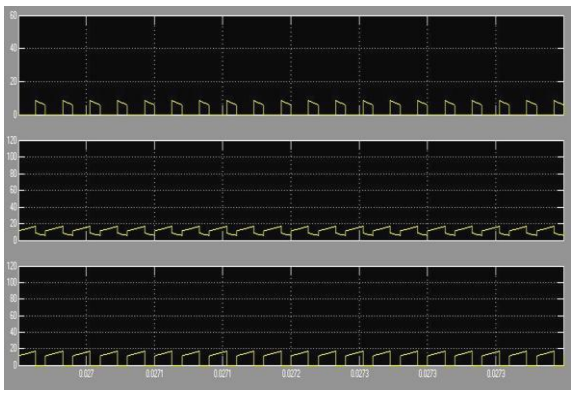

Figure 13: Waveforms of iD4, *i*in, *i*D3

International Research Journal of Innovations in Engineering and Technology (IRJIET)

ISSN (online): 2581-3048

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https://doi.org/10.47001/IRJIET/2021.504006

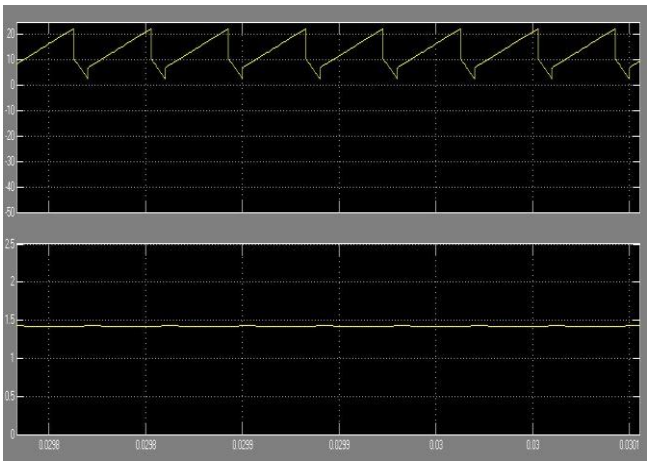

Figure 14: Waveforms of iS1& iD1

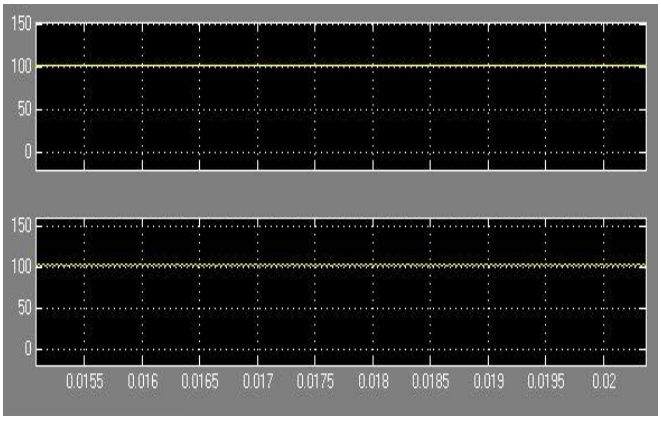

Figure 15: Voltage waveform across capacitors C1 & C2

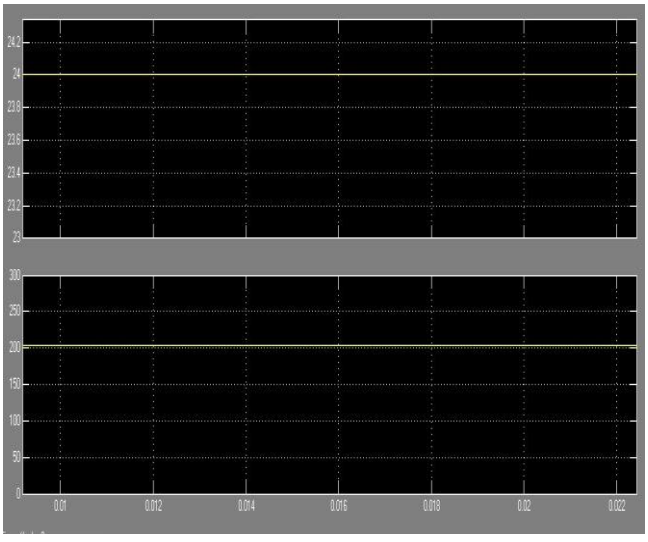

Figure 16: Waveforms of input & output voltages

When output power is over 70w, the proposed converter has higher efficiency than the conventional converter from the below figure. Also the measured efficiency of the proposed converter is 95.8% at the full condition.

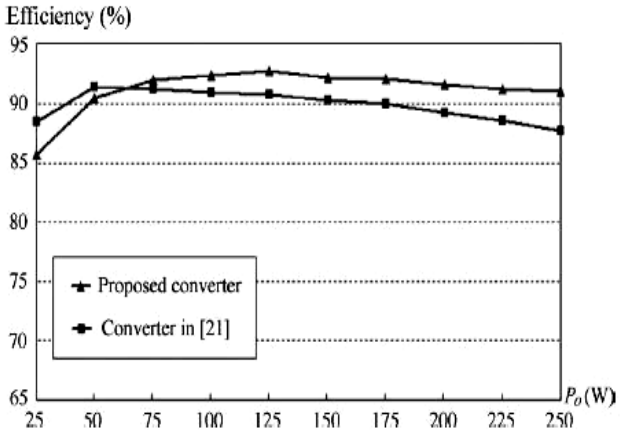

Figure 17: Measured efficiency of proposed converter and conventional converter with various output power

V. CONCLUSION

High step up dc-dc converter has been presented. The coupled inductor and voltage doubler circuits are integrated in the proposed converter to achieve high step-up voltage gain. And the energy stored in the leakage inductor of the coupled inductor is recycled. Voltages across the switches are half the level of the output voltage. Finally the proposed converter is modelled and efficiency is improved.

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ISSN (online): 2581-3048
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Citation of this Article:

Kondaparthy. Laxmi Krishna, "Coupled-Inductor and Voltage-Doubler Circuits with High Step-Up DC-DC Converter" Published in *International Research Journal of Innovations in Engineering and Technology - IRJIET*, Volume 5, Issue 4, pp 32-41, April 2021. Article DOI https://doi.org/10.47001/IRJIET/2021.504006

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