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Design of 16bit 6t SRAM Using Different CMOS Technologies Using Cadence Virtuoso Tool

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Abstract – Static Random Access Memory (SRAM) has been an important memory device in VLSI circuits. SRAM is used widely because of its huge storage capacity and can be accessed in less time with low power consumption. This paper presents design and implementation of 16Bit 6T SRAM using different CMOS technologies using Cadence Virtuoso tool. Due to the requirement of more storage, usage of 16-bit SRAM is convenient. The performance analysis of SRAM with respect to Power Dissipation and Average Delay is observed and compared.

Key Words: SRAM, 6T, CMOS, Power dissipation, Average Delay

1. INTRODUCTION

Static Random Access (SRAM) constitutes a large percentage of area in the VLSI designs due to the high number of transistors for a single SRAM cell. Thus, the SRAM cell generally employs a minimum size transistor to have a high packing density the size of the SRAM cell is being reduced using scaling over the past three decades.

SRAM takes two design aspects: the power dissipation and propagation delay in reading and writing the value into the SRAM cell. The power dissipated during read and write operation is dynamic power dissipation. It helps to determine the battery life of portable devices. The speed of SRAM is determined by the delay in reading and writing.

1.1 CMOS

Complementary Metal oxide Semiconductor (CMOS) is a technology used to produce integrated circuits. CMOS circuits are found in several types of electronic components, including microprocessors, batteries and digital camera image sensors. CMOS circuits offer much smaller power dissipation and almost no static power dissipation, CMOS transistor consists of P channel MOS (PMOS) and N channel MOS (NMOS).

Different Technologies of CMOS indicate the minimum gate length of the transistors, for example 45nm technology that means transistor gate length in this technology is 45nm and same with corresponding technologies

1.2 POWER DISSIPATION

Power dissipation can be defined as the product of total current supplied to the circuit and the total voltage loss or leakage current. Power dissipation in CMOS circuits is categorized in two types i.e., dynamic power and static power. Dynamic power is due to the switching behavior of the transistor which is charging and discharging of load capacitance. Static power dissipation is due to the leakage current produces continuously from the power supply.

Power dissipation can be minimized by different techniques, Low power supply voltage (VDD) is one of the most widely used technique to achieve low power dissipation.

2. 6T SRAM

6T SRAM consist of 6 transistors (MOSFET). Where 4 transistors are coupled as CMOS inverter, here bit is stored as 1 or 0 and other two transistors is act as pass transistor to control the SRAM cell by bits line. When WL (word line) is high then the SRAM cell can be accessed.

2.1 Read mode

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In read mode WL is selected and it enables the two pass transistors which are connected to the bit lines. Now the value stored at node A and B are transferred to the bit lines.1st assume 1 is stored at node so they will discharge through the N1 and the BL is pull up through P1 to VDD. In this mode of operation P1 and N2 transistors are turned off but the transistors N1 and P2 are operate in linear mode.

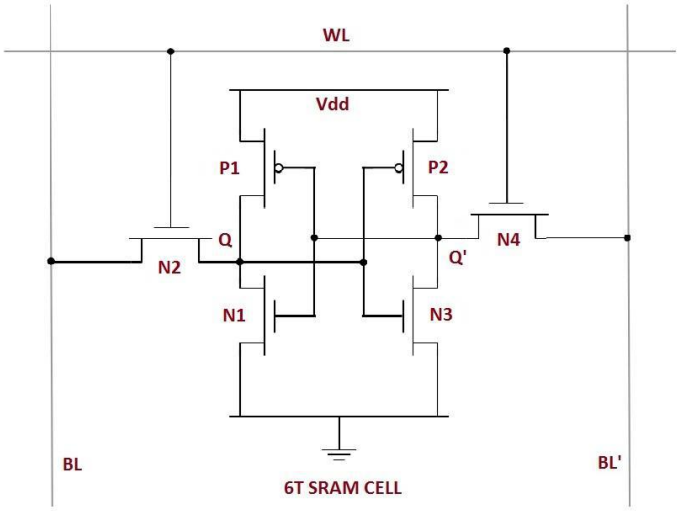

Fig 1: 6T SRAM cell

2.2 Write mode

In this mode and BL is charged to Vdd. To written something in SRAM either and BL is discharge to ground. If 1 is need to write BL is charged to Vdd and is discharged through ground. If logic 0 has to written charged to Vdd and BL is discharge through ground, then the WL gets active and data is written in to the cell.

3. DESIGN OF 6T SRAM CELL IN 180 NM, 90NM AND 45NM TECHNOLOGY

6T SRAM cell has been designed in 180 nm, 90 nm and 45 nm technology using Cadence Virtuoso tool which are shown in Fig.2, Fig.3,Fig.4 ,Fig.5.

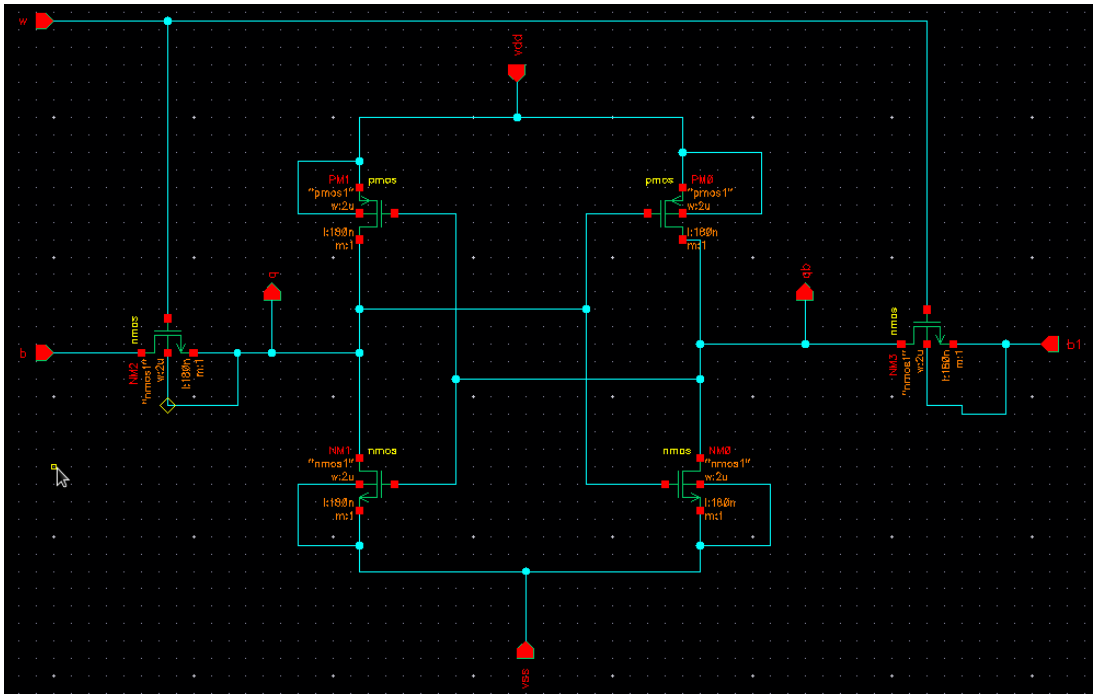

Fig 2. Schematic diagram of 6T SRAM cell in 180nm technology

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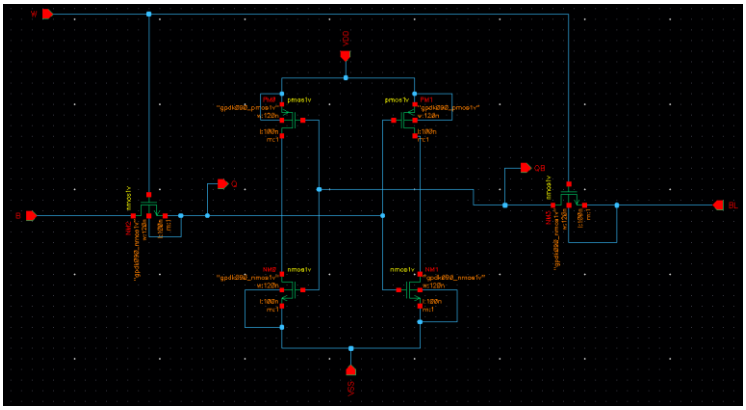

Fig 3. 6T SRAM cell in 90nm technology

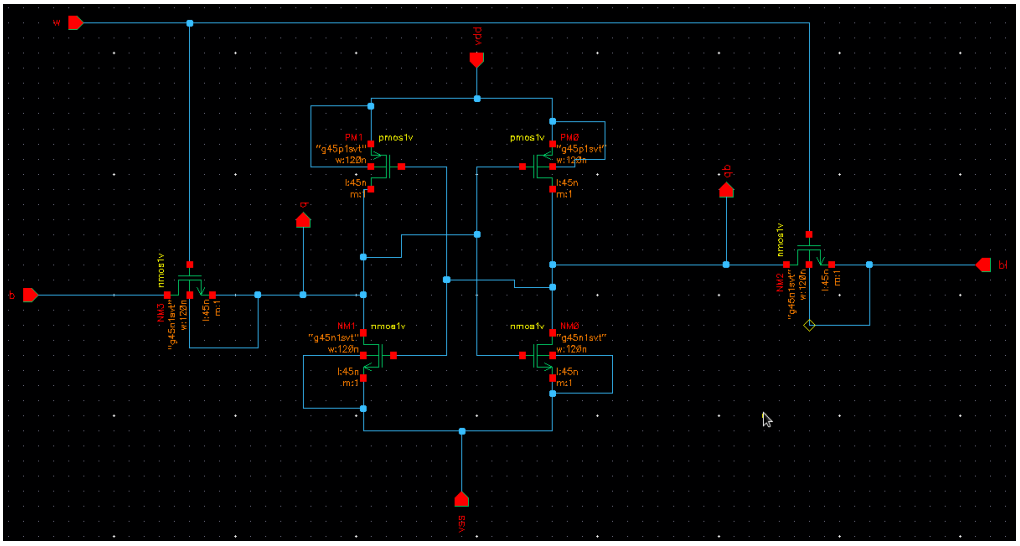

Fig 4. 6T SRAM cell in 45nm technology

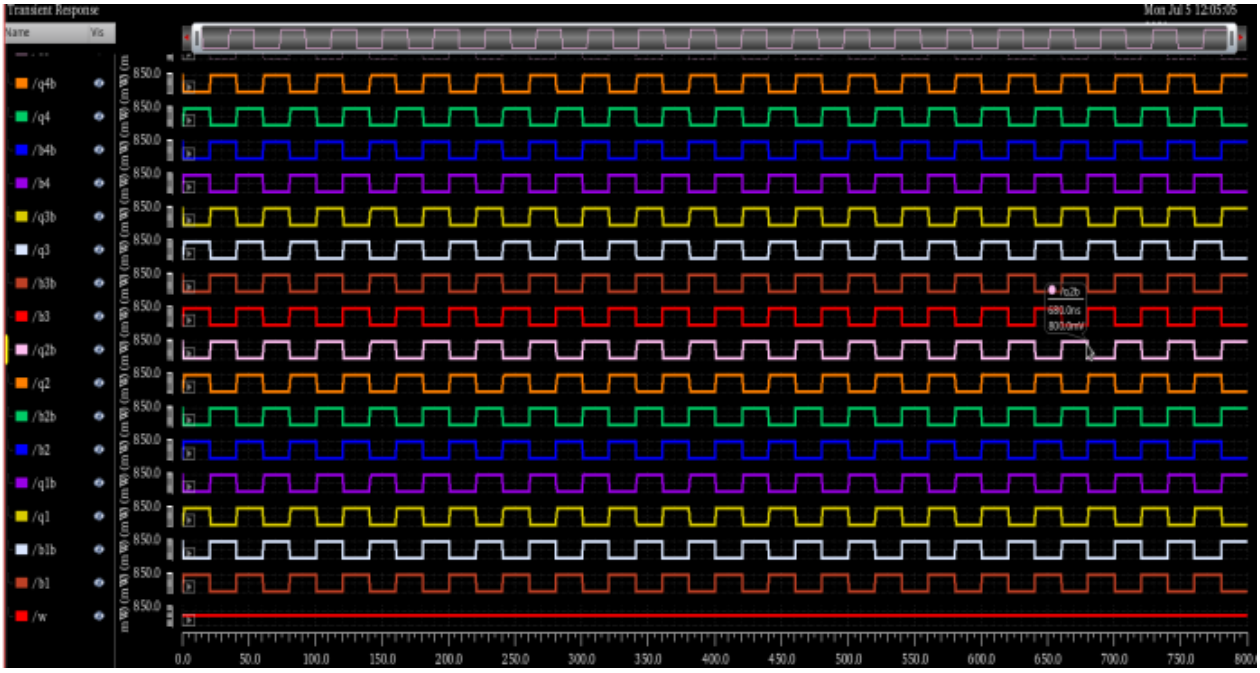

Fig 5. Waveform of 16-bit SRAM

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In this design, we have used supply voltage of 800mV and Write Input with lower and higher voltage of 0V and 800mV respectively.

4. DELAY ANALYSIS

Delay for each 6T SRAM cell in 180nm, 90nm and 45nm technology has been calculated and shown in Table 1. Delay time depends on the critical voltage and W/L ratio of the transistors.

Table 1: Delay time analysis

Technology	T rise	T fall	Average delay
180nm	231.4 ps	86.63 ps	157.31 ps
90nm	177.7 ps	20 ps	98.85 ps
45nm	14.72 ps	12.15 ps	13.43 ps

5. RESULT OF POWER DISSIPATION

It is the rate of energy which is consumed from the source and converted into heat. Dynamic power is due to the switching behavior of the transistor which is charging and discharging of load capacitance.

Power dissipation can be minimized by different techniques; Low power supply voltage (VDD) is one of the most widely used technique to achieve low power dissipation. When low supply voltage is applied to SRAM it improves battery life.

Table 2: Power Dissipation

Technology	Power
180 nm	106.4 uW
90 nm	1.226 uW
45 nm	464 nW

6. CONCLUSION

This paper presents 6T SRAM memory design of 16-bit storage, in different nodes. The performance evaluation of all 3 designs was carried out. The performance criteria were total power dissipation & average delay. It was observed that reduction in technology results in reduced power dissipation & average delay. The comparison of the results is done at 180nm, 90nm, 45nm technology nodes. It shows that power dissipation and average delay is improved as the channel length is reduced.

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