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Comparison of Different Types of SPWM Techniques for Single Phase 31 Level Cascaded H-Bridge Inverter

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***Abstract* - Multilevel inverters have been regarded as a superior choice for medium voltage and high power applications because they have good waveform quality, higher performance, and are made up of switching devices that are subjected to minimal pressures. The multilevel inverter is used to reduce harmonics to improve voltage quality. As the multilevel inverter's voltage levels increase, harmonics are reduced as well, which considerably reduces losses. This paper discusses the Level Shifted Carriers Based Pulse Width Modulation (LS-PWM) and phase-shifted carriers pulse width modulation (PS-PWM) Techniques for Single Phase inverters 31 levels. LSPWM is divided into three subgroups: phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD). Simulation data are obtained using MATLAB / SIMULINK. Results show (PS-PWM) has less THD in output wave voltage than (LS-PWM).**

Keywords: Multilevel inverter, Sinusoidal pulse width modulation (SPWM), Total Harmonic Distortion (THD), phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD).

I. INTRODUCTION

The primary purpose of the inverter is to convert a dc source voltage to an ac voltage [1]. Consumer and industrial applications both frequently use inverters [2]. In general, two-level inverters produce more harmonics, which leads to higher losses and heat issues in the machine, which wear down the insulation protecting the conductors and lower motor efficiency [3,4]. Multilevel inverters are designed to reduce harmonic distortion in the output waveform and enhance the performance of the entire system in terms of harmonics, DV/DT pressures, and pressures on a motor's bearings [5]. A multilevel inverter is a device that combines semiconductors and voltage sources to produce a waveform with stepped output voltage. Inverter output voltage levels are dependent on the number of input DC voltage levels, and as levels rise, harmonics are minimized. Multilevel inverter architectures are becoming more common. There are a number of multilevel converter topologies that have been created, including diode clamped, flying capacitors, and cascaded H-bridge [6]. Cascaded multilevel inverters are widely utilized in electric vehicle applications, active power filters, motor drives, power factor correction devices, var compensators, grid interfacing with renewable energy sources, and so on [7].

A cascaded multilevel inverter is made up of a number of H-bridge inverters, also known as single-phase full bridge inverters [8]. Each H-bridge unit has a separate dc source, and each H-bridge may generate three different voltage levels: +V, 0V, and -V by connecting the de source to the ac output side using various combinations of the four switches S1, S2, S3, and S4 of one H-bridge and S5, S6, S7, and S8 of another H-bridge[9]. Each H-ac bridge's output is linked in series, resulting in a synthetic output voltage waveform that is the total of all of the outputs from each H-bridge [10]. The connecting diagram for a single phase cascaded inverter is shown in Figure 1.

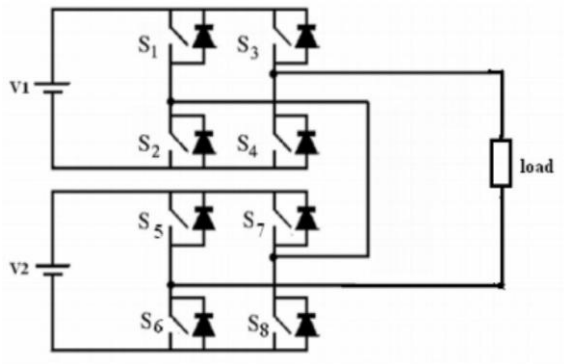

Figure 1: Single phase cascaded multilevel inverter

II. PWM TECHNIQUE

As various multilevel inverter designs are offered, numerous modulation approaches and control paradigms such as SPWM, SHE-PWM (selective harmonic elimination), SVM (space vector modulation), and others have been [11]. SPWM is the simplest approach for implementing inverters. [12]. The SPWM principle is illustrated here, where a sinusoidal modulating wave is compared to a triangular carrier wave to provide two states (high or low). If the modulating wave amplitude is greater than the amplitude of the carrier wave, the state is high; otherwise, the state is low. When the switch is in

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the high state, it turns on, and when it is in the low state, it turns off [13]. The SPWM technique is used to manage the switching pattern of an inverter, resulting in a lower THD for output voltage. The multi carrier PWM approach is used to manage the switching pattern of multilevel inverters. Carrier-based PWM approaches for MLIs are categorized as [14,15]:

1. Single Carrier SPWM
2. Multi Carrier SPWM

For m - level CHB inverter, (m - 1) carrier waves are required for multi carrier SPWM approach[16]. All carrier waves must have the same amplitude and frequency. The Multi - Carrier PWM control techniques are further classified as follows:

1. Phase shifted
2. Level shifted

A) Phase Shifted SPWM

Phase shift carrier PWM is a technique of PWM theories that use a constant switching frequency. All triangular carriers in this PWM scheme have the same frequency and peak amplitude [17]. However, any two adjacent carrier waves undergo a phase change, as shown by:

$$\Theta=360/(m-1)$$

Where Θ is phase angle between any two carrier waves and m is the number of voltage level as shown on in Figure 2.

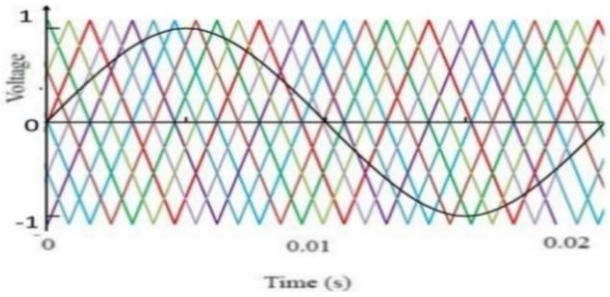

Figure 2: Phase Shifted Control Scheme

B) Level Shifted SPWM

This technique is divided into three types:

1. Phase Disposition (PD)
2. Phase Opposition Disposition (POD)
3. Alternate Phase Opposition Disposition (APOD)

1. Alternate Phase Opposition Disposition (APOD): A method in which the adjacent two triangular carrier signals are mirrored. These adjacent two carrier waves being displaced by 180[18].as shown in figure 3.

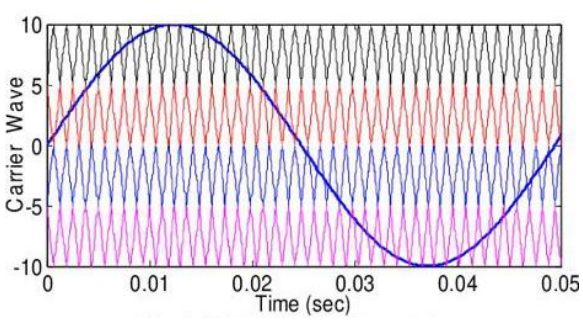

Figure 3: APOD Control Scheme

2. Phase Opposition Disposition (POD): A method in which the carrier signals above zero are in phase, while the carrier signals below zero are in opposing phase to the triangle signals above zero. If 0 level is considered the mirror, it appears to be a mirror image [19]. As shown in figure 4.

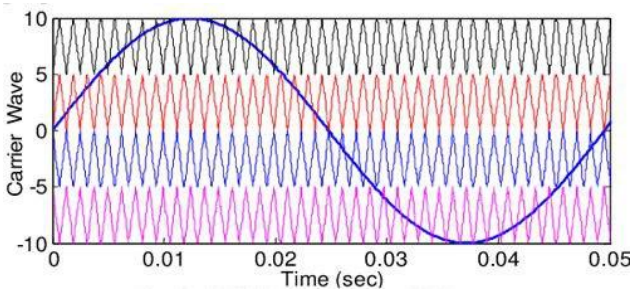

Figure 4: POD Control Scheme

3. Phase Disposition (PD): A method in which the triangle carrier signals above and below zero levels are in phase but only the level is modified [20].as shown in figure 5.

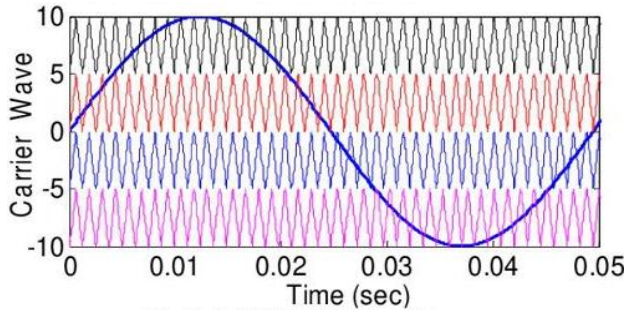

Figure 5: PD Control Scheme

III. SIMULATION RESULTS

The MATLAB / Simulink model of a 31 Level- Cascaded H - Bridge Inverter is shown in Figure 9. It necessitates the use of four H - bridges, each of which is made up of four MOSFET switches and four DC voltage sources V1, V2, V3, and V4. The DC sources are chosen in a 1:2:4:8 ratios and the circuit's input voltages are V1=21 V, V2=42V, V3=84V, and V4=168V, respectively. This circuit can produce stepped wave that contain 31 level as shown in figure (10).

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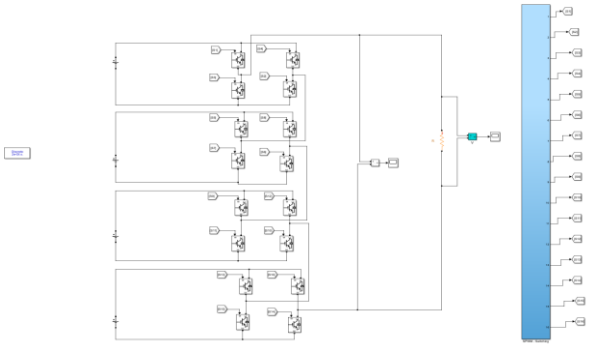

Figure 9: Simulation model of 31 Level-Cascaded H-Bridge inverter

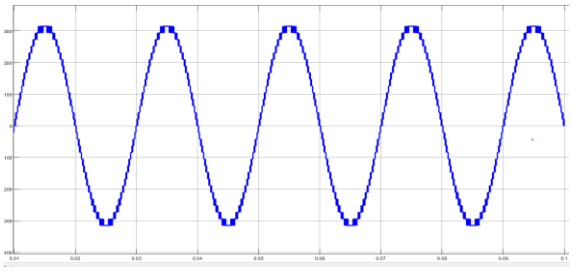

Figure 10: Illustrate output wave voltage for 31 levels

Figure 11 demonstrates the equivalent output voltage waveform's harmonic spectrum. Using PD-SPWM, THD is around 3.76%.

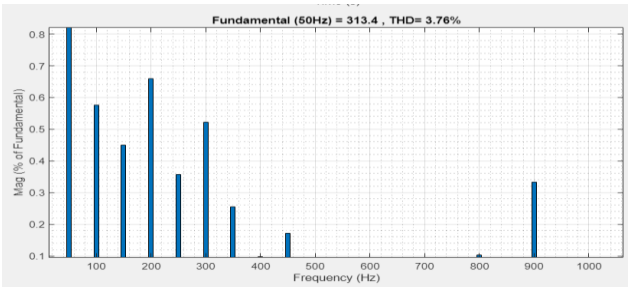

Figure 11: FFT analysis of 31 Level-Cascaded H-Bridge inverter using PD-SPWM

Figure 12 represents the equivalent output voltage waveform's harmonic spectrum. Using POD-SPWM, %THD is nearly 3.79%.

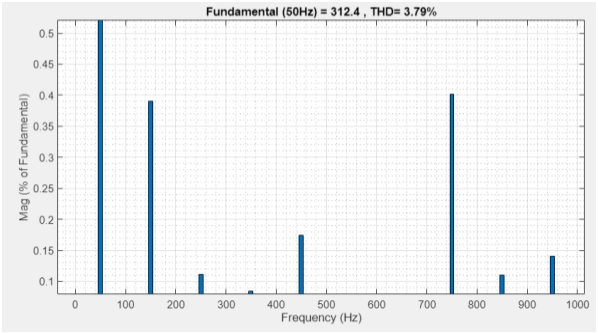

Figure 12: FFT analysis of 31 Level-Cascaded H-Bridge inverter using POD-SPWM

Figure 13 shows the equivalent output voltage waveform's harmonic spectrum. Using APOD-SPWM, %THD is nearly 3.88%.

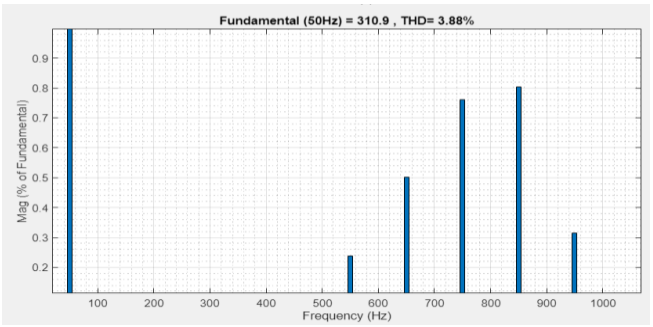

Figure 13: FFT analysis of 31 Level-Cascaded H-Bridge inverter using APOD-SPWM

Figure 14 represents the equivalent output voltage waveform's harmonic spectrum. Using PS-SPWM, %THD is nearly 3.79%.

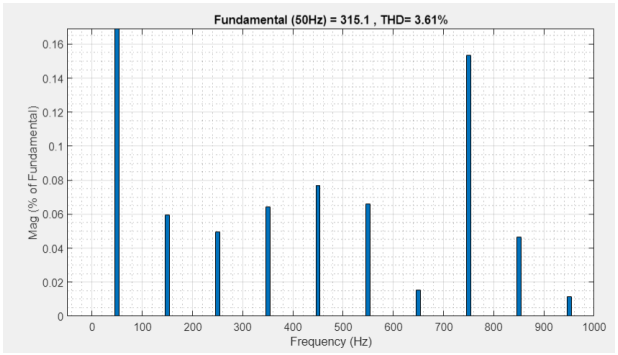

Figure 14: FFT analysis of 31 Level-Cascaded H-Bridge inverter using PS-SPWM

Table 1: Vrms and THD for 31-level

	Level Shifted			Phase shifted
	PD-SPWM	POD-SPWM	APOD-SPWM	
THD%	3.76	3.79	3.88	3.61
Vrms	221.6	220.9	219.7	222.8

IV. CONCLUSION

This paper offers an MLI with four asymmetric H-bridge DC sources produce 31 level in output voltage. The suggested inverter's main purpose is to demonstrate the comparison of LS SPWM and PS - SPWM control approaches in order to obtain a multilevel inverter with fewer switching components and reduced total harmonic distortion (THD). Matlab was used to simulate various SPWM techniques. And percentage THD of output voltage is analyzed through FFT analysis. The results findings show that the voltage total harmonic distortion (THD) in phase shift PWM is fewer than level shift PWM.

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