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Profile-Aware Parasitic Extraction of Tapered Through-Glass Vias: Quantifying the Validity of the Ideal-Cylinder Compact Model

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***Abstract* - Through-glass vias (TGVs) are the vertical interconnect of choice for emerging glass-substrate 2.5-D and 3-D packaging, yet fabricated vias are not ideal cylinders: laser and etch-based processes leave a tapered profile, while the compact equivalent-circuit models used in fast channel simulation almost universally assume a straight cylindrical via. This work quantifies, from full-wave simulation, how the extracted parasitics of a coaxial TGV depend on taper and establishes the range over which the ideal-cylinder assumption remains accurate. A parametric three-dimensional model is solved with a full-wave transient solver over a factorial sweep of taper ratio, top diameter, and glass thickness; series resistance and inductance and shunt capacitance are extracted from the simulated admittance parameters using an asymmetry-robust formulation. A Gaussian-process surrogate trained on the resulting dataset reproduces the full-wave parasitics under leave-one-out cross-validation with a coefficient of determination of at least 0.97, enabling dense exploration of the design space at negligible cost. The series inductance increases monotonically as the via tapers, by about thirteen percent over the studied range, and the ideal-cylinder model is shown to remain within a ten percent inductance error only down to a taper ratio of about 0.68, below which a profile-aware correction is required.**

Keywords: Through-glass via, glass packaging, parasitic extraction, equivalent-circuit model, signal integrity, Gaussian process, surrogate model.

I. INTRODUCTION

Glass substrates are gaining rapid traction for 2.5-D and 3-D heterogeneous integration because of their low dielectric loss, dimensional stability, and panel-level scalability relative to silicon interposers [1], [2]. In these substrates the vertical interconnect is the through-glass via (TGV), whose high-frequency behavior increasingly limits signal integrity as data rates rise. Recent work characterizing the parasitic RLGC of high-density TGVs shows that parasitic inductance is a primary driver of impedance mismatch and signal delay [3], and measurements on glass-package test vehicles confirm that interconnect resonances degrade signal and power integrity [2].

A practical complication is that fabricated TGVs are seldom ideal cylinders. Laser-induced and wet-etch processes produce vias with a tapered profile, so the top and bottom diameters differ. Yet the compact equivalent-circuit models embedded in fast channel- and system-level simulators are almost always derived for a straight cylindrical via. The dependence of the extracted compact-model parameters on taper and the range over which the ideal-cylinder assumption stays accurate are not well quantified.

This paper addresses that gap. Using full-wave time-domain simulation of a coaxial TGV, we (i) extract the series resistance and inductance and the shunt capacitance of the via as a function of taper, top diameter, and glass thickness; (ii) train a Gaussian-process surrogate on the resulting dataset so the design space can be mapped densely; and (iii) determine the taper threshold below which the ideal-cylinder inductance is no longer representative. The contribution is a profile-aware view of TGV parasitics and a concrete validity bound for the conventional compact model.

II. STRUCTURE AND SIMULATION SETUP

2.1 Geometry and Material

The modeled structure, shown in Figure 1, is a single signal passing through a glass slab, enclosed by a coaxial copper ground wall that provides the return path. The via is a truncated cone of top diameter D_{top} and bottom diameter $D_{bot} = \tau$ x D_{top}, where the taper ratio $\tau = D_{bot}/D_{top}$ equals unity for a straight cylinder. The glass thickness is h. The dielectric is Schott FOTURAN II photostructurable glass, modeled with the dispersive material data from the simulator material library; the manufacturer data are characterized to about 5 GHz and extended by an analytic dispersion model above that. The relative permittivity and loss tangent are ε_r = 6.40 and tan δ = 0.0109 (at 5 GHz), extended above 5 GHz by

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a second-order Debye dispersion model fitted to the manufacturer data (fit error ≈ 9.3×10^{-4}).

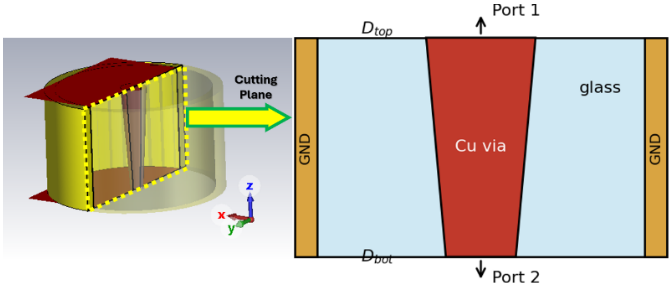

Figure 1: Cross-section of the tapered coaxial through-glass via

2.2 Solver and Excitation

The structure is excited by coaxial waveguide ports on the top and bottom faces and solved with the transient (time-domain) solver on a hexahedral PBA mesh of about 4.9×10^5 cells over 1–40 GHz [7]. Electric boundary conditions enclose the domain, consistent with the surrounding ground wall. Each solve produces the two-port scattering matrix, exported as a Touchstone file.

2.3 Parametric Sweep

Three geometric variables are swept in a full-factorial design: taper ratio τ in {0.6, 0.7, 0.8, 0.9, 1.0}, top diameter D_{top} in {30, 50, 70} µm, and glass thickness h in {100, 200, 300} µm. Of the 45 nominal combinations, 41 are used in this study. Each run is exported automatically, yielding one Touchstone file per parameter combination.

III. PARASITIC EXTRACTION

For each run, the simulated two ports are reduced to a lumped R-L-C description. Because a tapered via is geometrically asymmetric, a symmetric pi assumption is inaccurate at low frequency; the parasitics are therefore extracted directly from the admittance parameters. The series impedance of the via is

$$Z_s = -1/Y21 = R + j\,w\,L \qquad (1)$$

from which R is the real part of Z_s and L is the imaginary part of Zs divided by the angular frequency. The shunt admittance, averaged over both ports to absorb the top-bottom asymmetry, is

$$Y_{sh} = \frac{1}{2}[(Y_{11} + Y_{21}) + (Y_{22} + Y_{21})] = G + j\,w\,C \; (2)$$

The series resistance and inductance are read in a low-frequency band (0.5 to 2 GHz) where they are stable. The shunt term is ill-conditioned at low frequency for this series-dominated, asymmetric element, so the capacitance is read in a converged higher band (15 to 25 GHz). The shunt conductance is dominated by numerical noise for this low-loss glass via and is not retained as a modeling target; the compact model is accordingly R-L-C.

IV. SURROGATE MODEL

To map the parasitics continuously over the design space without a full-wave solve at every point, a Gaussian-process regression surrogate is trained on the 41-run dataset, with inputs (τ, D_{top}, h) and a separate model per parasitic target. Gaussian-process regression is well suited to tens of expensive samples in a few dimensions and provides predictive uncertainty [5], [6]; the chosen design size is consistent with established guidance for computer experiments [4]. An anisotropic Matern-5/2 kernel with a noise term is used, and inputs are standardized. Given the small sample, model quality is assessed by leave-one-out cross-validation rather than a single hold-out split.

V. RESULTS AND DISCUSSIONS

5.1 Taper Dependence of the Parasitics

Figure 2 shows the extracted series inductance versus taper for the three via diameters at h = 200 µm. Inductance increases monotonically as the via tapers for every diameter: at D_{top} = 50 µm it rises from 0.0727 nH at τ = 1.0 to 0.0822 nH at τ = 0.6, an increase of about 13 percent; the 30µm family shows a comparable trend. Physically, narrowing the lower part of the via reduces its effective cross-section and raises the series inductance. The shunt capacitance behaves oppositely and weakly, decreasing by a few femtofarads as τ decreases. The return loss also shifts with taper, but its direction depends on D_{top}, which simultaneously sets the coaxial line impedance, so it is treated here as a secondary observation.

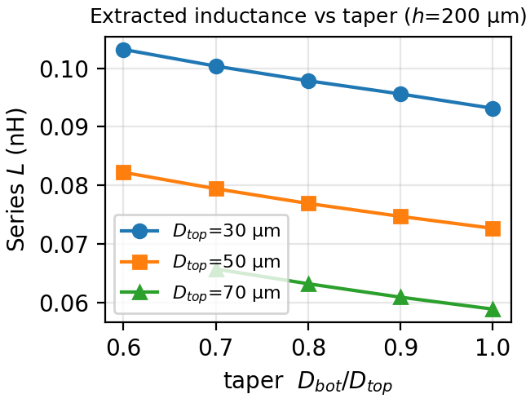

Figure 2: Extracted series inductance versus taper ratio for three via diameters (h = 200 µm)

5.2 Surrogate Accuracy

Table 1 reports the leave-one-out cross-validation accuracy of the surrogate for each parasitic target. The inductance and capacitance are essentially predicted exactly, the 20-GHz return loss to a coefficient of determination of 0.994, and the small series resistance, the most sensitive quantity, to 0.97. The high cross-validated accuracy also indicates that the 41-point design is sufficient: no additional runs are required. Figure 3 shows the leave-one-out prediction versus simulated inductance, with points lying on the ideal line. The trained surrogate evaluates a design point in well under a millisecond, versus about 2.4 minutes (143 s) per run for a full-wave solve of the same model ($\approx 4.9\times10^5$ mesh cells, six CPU threads) — roughly five orders of magnitude faster — enabling the dense mapof Figure 4. The remaining four were aborted by the solver and excluded.

Table 1: Leave-one-out cross-validation accuracy of the surrogate

Target	R-squared	RMSE
Inductance L	0.99997	0.0002 nH
Capacitance C	0.99946	0.20 fF
Return loss @20 GHz	0.99405	0.37 dB
Resistance R	0.96752	1.81 mΩ

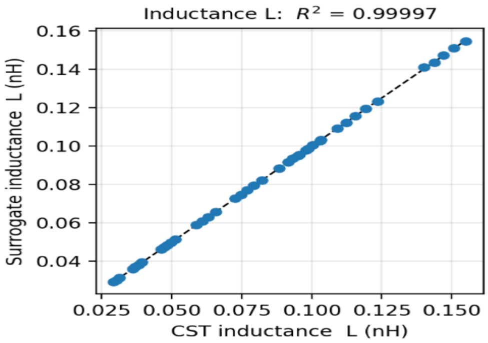

Figure 3: Leave-one-out cross-validation of the inductance surrogate (predicted vs full-wave)

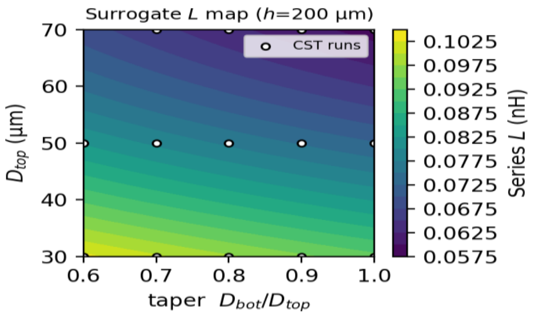

Figure 4: Surrogate-predicted series inductance over the taper and top-diameter plane

5.3 Validity of the Ideal-Cylinder Model

The central question is how far a model built for a straight via (τ = 1) can be trusted as the real via tapers. Figure 5 plots the deviation of the surrogate inductance from its ideal-cylinder value as a function of taper. The deviation grows monotonically as the via narrows and crosses a 10 percent tolerance at a taper ratio of about 0.68. In other words, for τ greater than about 0.68 the conventional ideal-cylinder compact model represents the via inductance within 10 percent, whereas for stronger tapers a profile-aware correction is necessary. This single bound is a practical design guideline.

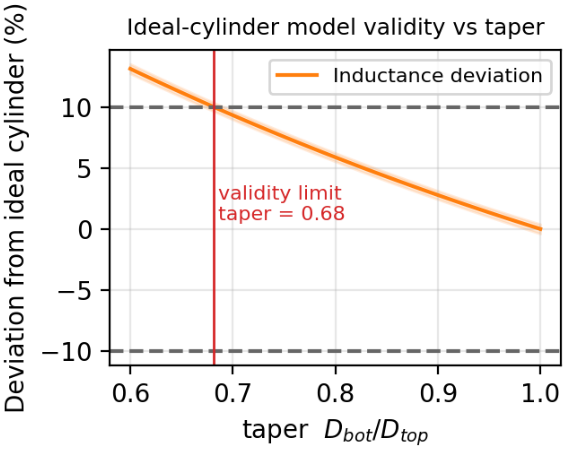

Figure 5: Deviation of the inductance from the ideal-cylinder value versus taper ratio

VI. CONCLUSION

We presented a profile-aware parasitic study of tapered through-glass vias. Series resistance and inductance and shunt capacitance were extracted from full-wave simulation over a factorial sweep of taper, via diameter, and glass thickness using an asymmetry-robust admittance-parameter formulation, and a Gaussian-process surrogate reproduced the parasitics under leave-one-out cross-validation with a coefficient of determination of at least 0.97. The series inductance rises monotonically, by up to about 13 percent, as the via tapers, and the conventional ideal-cylinder compact model is shown to remain within a 10 percent inductance error only down to a taper ratio of about 0.68. The resulting guideline lets designers decide when a straight-via model suffices and when the fabricated taper must be modeled explicitly. Future work will incorporate sidewall roughness and extend the surrogate to differential TGV pairs.

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